INSTRUCTION MANUAL

TYPE 1781 | DIGITAL LIMIT COMPARATOR

1781

GENERAL RADIO COMPANY

A

SPECIFICATIONS

RANGE OF LIMIT SETTINGS: 00000 to 19999 for both C and D.
ACCURACY: Same as that of data source.

INPUT

Data: 11 digits, BCD, 1–2–4–2 (1–2–4–8 optional).

Logic Levels:
"1" = V_{REF} (V_{REF} to $V_{REF}-2$ volts)
"0" = $V_{REF}-10$ ($V_{REF}-8$ to $V_{REF}-50$ volts).
Input Resistance: >47 kΩ (connected to V_{REF}).
Maximum Source Resistance: 100 kΩ.

Reference Voltage: ±50 V with respect to chassis ground. Maximum source resistance, 1 kΩ.

Compare Command: Logic 1 to logic 0 transition. Minimum duration, 2.5 ms; input resistance, >50 kΩ. Maximum source resistance, 20 kΩ.

OUTPUT

Data: Identical to input.

Comparison Result: BCD digit, behind 10 kΩ.

Print Command: Logic 1 to logic 0 transition, behind 2.2 kΩ.

Relay Contacts: 4 SPDT contacts, 115 V, rms, 0.1 A, rms, maximum.

GENERAL

Accessories Supplied: CAP-22 Power Cord, spare fuses, 4205–1000 Signal Cable to connect comparator to measuring instrument.
Accessories Required: If sorting equipment is used, 4205–1010 cable is also needed.
Power Required: 105 to 125 or 210 to 250 V. 50 to 60 Hz, 10 W. (195 to 235 also available.)
Cabinet: Rack-bench.
Dimensions: Bench model, width 19, height 4, depth 16½ in (485, 105, 420 mm) over-all; rack model, width 19, height 3½, depth behind panel 16 in (485, 89, 410 mm).
Net Weight: 20 lb (9.5 kg).
Shipping Weight: 30 lb (14.0 kg).

General Radio Experimenter, Nov-Dec 1966

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Form 1781-0100A GENERAL RADIO COMPANY
West Concord, Mass; USA.

CONDENSED OPERATING INSTRUCTIONS

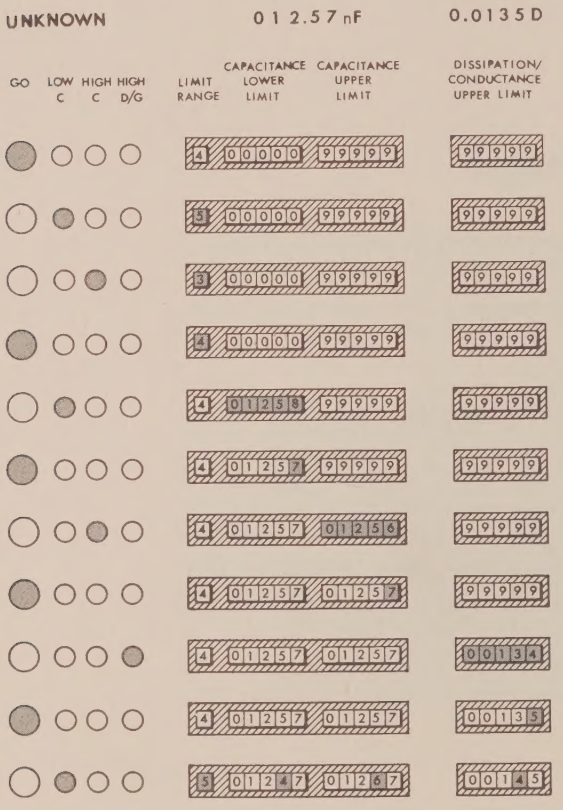
Referenced paragraphs contain unabridged instructions.

CAUTIONS: Be sure the line switch on the rear of the instrument is set for the proper line voltage.

Do not operate the instrument on its side unless the relay board is removed.

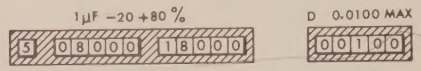
Turn off power before removing or replacing etched boards.

OPERATIONAL CHECKS EXAMPLE (3.1.2)



MULTIPLE-GROUP SORTING EXAMPLE (3.2.2)

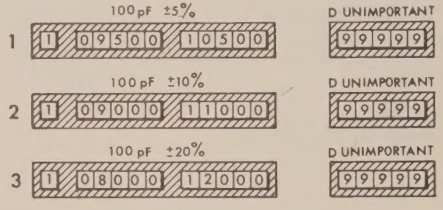
An incoming lot of nominal 1-μF capacitors is to be checked for a tolerance of −20 +80% and a maximum D of 0.0100.



Set LIMIT RANGE switch to 5 (from table below). Set CAPACITANCE LOWER LIMIT switches to 1μF − (0.2 x 1μF) = 08000 and CAPACITANCE UPPER LIMIT switches to 1μF + (0.8 x 1μF) = 18000. Set DISSIPATION/CONDUCTANCE UPPER LIMIT switches to 00100.

MULTIPLE-LIMIT SORTING EXAMPLE (3.2.3)

A production lot of nominal 100-pF capacitors is to be sorted into categories of ±5%, ±10%, ±20%, and over 20%. Dissipation factor is unimportant.



Set rear-mounted DATA READY COMMAND CONTROLS to PRINT-OUT-OF-TOLERANCE only and set LIMIT RANGE switch to 1 (from table below). Set DISSIPATION/CONDUCTANCE UPPER LIMIT switches to 19999.

Comparator 1: Set CAPACITANCE LOWER LIMIT switches to 100pF - (0.05 x 100pF) = 09500 and CAPACITANCE UPPER LIMIT switches to 100pF +(0.05 x 100pF) = 10500.

Comparator 2: Set CAPACITANCE LOWER LIMIT switches to 100pF - (0.1 x 100pF) = 09000 and CAPACITANCE UPPER LIMIT switches to 100pF +(0.1 x 100pF) = 11000.

Comparator 3: Set CAPACITANCE LOWER LIMIT switches to 100pF - (0.2 x 100pF) = 08000 and CAPACITANCE UPPER LIMIT switches to 100pF + (0.2 x 100pF) = 12000.

RANGE INFORMATION FOR TYPE 1680-A AUTOMATIC CAPACITANCE BRIDGE ASSEMBLY

RANGE	CAPACITANCE		LOSS	
	120 c/s MAX	*400 c/s, 1 kc/s* MAX	*CONDUCTANCE* MAX	*DISSIPATION FACTOR* MAX
1		150.00pF	1500.0n℧	1.5000 D
2		1500.0pF	15.000μ℧	1.5000 D
3		15.000nF	150.00μ℧	1.5000 D
4	1500.0nF	150.00nF	1500.0μ℧	1.5000 D
5	15.000μF	1500.0nF	15.000m℧	1.5000 D
6	150.00μF	15.000μF	150.00m℧	1.5000 D
7	1500.0μF	150.00μF	1500.0m℧	1.5000 D

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1.1 PURPOSE

The Type 1781 Digital Limit Comparator is used in conjunction with the Type 1680-A Automatic Capacitance Bridge Assembly to sort capacitors to preset limits. The comparator provides a visual GO-NO GO readout and corresponding output data for recording and control. The comparator and bridge comprise the measurement and control equipment for a completely automatic sorting system, which is equally useful in manual and semi-automatic sorting. Capacitor manufacturers can use it for production testing, capacitor users for incoming inspection.

1.2 DESCRIPTION

The comparator is a sequential calculator, which automatically compares the input BCD data (from the automatic capacitance bridge) with preset limits for both capacitance and loss.

Front panel thumb-wheel switches set:

limit range
capacitance lower limit
capacitance upper limit
dissipation factor/conductance upper limit

Front panel lamps indicate:

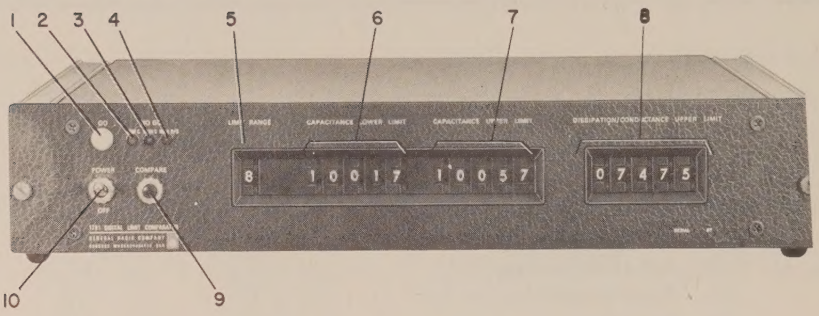
within tolerance – GO
C_X > upper limit – HIGH C
C_X < lower limit – LOW C
D_X or G_X > upper limit – HIGH D/G

The BCD data output will operate another comparator, a printer, or a number of other recording or data-processing devices. The relay contacts can actuate automatic sorting devices. When the BCD output is used to actuate the Type 1137 Data Printer, capacitance and loss values, as measured by the Type 1680-A Automatic Capacitance Bridge Assembly, are printed; in-tolerance units are in black, out-of-tolerance in red. The printer mode can be set from the rear of the comparator to print only in-tolerance units, out-of-tolerance units, or both.

1.3 ACCESSORIES SUPPLIED

	Qty	*Description*	*Part Number*
	1	Instruction manual	1781-0100
	1	Power cord, Type CAP-22	4200-9622
	1	Fuse, 0.25 A	5330-0700
	1	Fuse, 0.125A	5330-0450
	1	Universal cable	4250-1000
Bench model:	1	End frame set	5310-9624
Rack model:	1	Rack support set	7863-9624

1.4 FRONT PANEL



1 GO – Incandescent lamp with white filter. Lights when comparison result is GO (in tolerance).

2 LOW C – Incandescent lamp with red filter. Lights when comparison result is NO GO (out of tolerance) due to a capacitance value which is below the limit set by the LIMIT RANGE and CAPACITANCE LOWER LIMIT switches.

3 HIGH C – Incandescent lamp with red filter. Lights when comparison result is NO GO (out of tolerance) due to a capacitance value which is above the limit set by the LIMIT RANGE and CAPACITANCE UPPER LIMIT switches.

4 HIGH D/G – Incandescent lamp with red filter. Lights when comparison result is NO GO (out of tolerance) due to a capacitor dissipation factor or conductance which is above the limit set by the DISSIPATION/CONDUCTANCE UPPER LIMIT switches.

5 LIMIT RANGE – Single ten-position thumb-wheel switch. Sets the range for the capacitance values:

RANGE INFORMATION FOR TYPE 1680-A AUTOMATIC CAPACITANCE BRIDGE ASSEMBLY

RANGE	VOLTAGE	CAPACITANCE				LOSS			
		120 c s		400 c s, 1 kc s		CONDUCTANCE		DISSIPATION FACTOR	
	rms, across UNKNOWN	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
1	1 V			000.01 pF	150.00 pF	0000.1 n℧	1500.0 n℧	0.0000 D	1.5000 D
2	1 V			0150.0 pF	1500.0 pF	01.500 μ℧	15.000 μ℧	0.0000 D	1.5000 D
3	1 V			01.500 nF	15.000 nF	015.00 μ℧	150.00 μ℧	0.0000 D	1.5000 D
4	1 V	0000.1nF	1500.0nF	015.00 nF	150.00 nF	0150.0 μ℧	1500.0 μ℧	0.0000 D	1.5000 D
5	100 mV	01.500μF	15.000μF	0150.0 nF	1500.0 nF	01.500 m℧	15.000 m℧	0.0000 D	1.5000 D
6	10 mV	015.00μF	150.00μF	01.500 μF	15.000 μF	015.00 m℧	150.00 m℧	0.0000 D	1.5000 D
7	1 mV	0150.0μF	1500.0μF	015.00 μF	150.00 μF	0150.0 m℧	1500.0 m℧	0.0000 D	1.5000 D

6 CAPACITANCE LOWER LIMIT – Five ten-position thumb-wheel switches. Set the lower limit for the capacitance values.

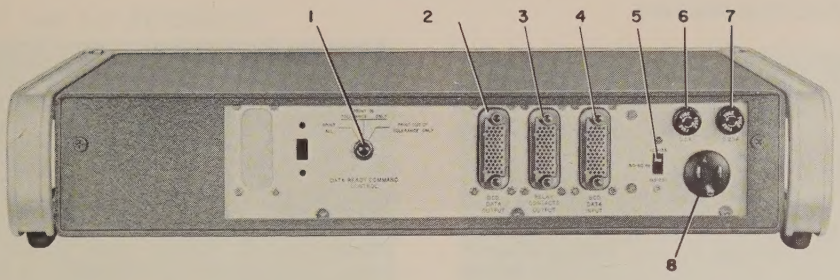
7 CAPACITANCE UPPER LIMIT – Five ten-position thumb-wheel switches. Set the upper limit for the capacitance values.

8 DISSIPATION/ CONDUCTANCE UPPER LIMIT – Five ten-position thumb-wheel switches. Set the upper limit for the dissipation-factor or conductance-values.

9 COMPARE – Push-button switch. Initiates comparisons manually if data source is ready (has completed a measurement).

10 POWER – Two-position toggle switch. Applies line voltage to the instrument.

1.5 REAR PANEL



1 **DATA READY COMMAND CONTROL** — Three-position screwdriver-operated rotary switch. Controls operation of external equipment connected to BCD DATA INPUT socket as follows:

PRINT ALL. External equipment operates after each comparison.

PRINT IN-TOLERANCE ONLY. External equipment operates only after a GO comparison.

PRINT OUT-OF-TOLERANCE ONLY. External equipment operates only after a NO GO comparison.

2 **BCD DATA OUTPUT** — 52-pin socket. Parallel connections from BCD DATA INPUT socket so that measurement data can be used by a recorder, digital-to-analog converter, another comparator, or other data processing equipment.

3 **RELAY CONTACTS OUTPUT** — 52-pin socket. Provides control signals to external sorting equipment.

4 **BCD DATA INPUT** — 52-pin socket. Measurement data input to comparator from Type 1680-A Automatic Capacitance Bridge Assembly or other data source.

5 **line** — Two-position screwdriver-operated slide switch. Selects line voltage range; 105 to 125V, 195 to 235V, or 210 to 250V, 50 to 60 Hz, 10W.

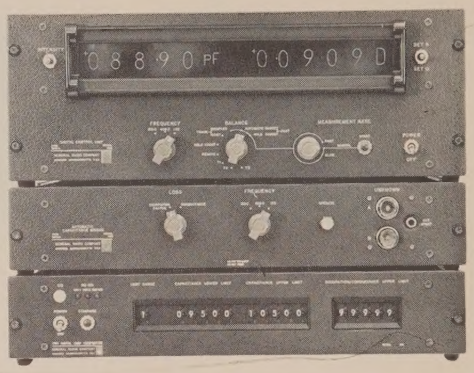
6 **fuse** — Fuse, 0.25A 3AG Slo-Blo for 105-to-125-V operation.

7 **fuse** — Fuse, 0.125A 3AG Slo-Blo for 195-to-235-V operation.

8 **power connector** — Three-pin male connector. For connection to power line. Accepts Type CAP-22 Power Cord.

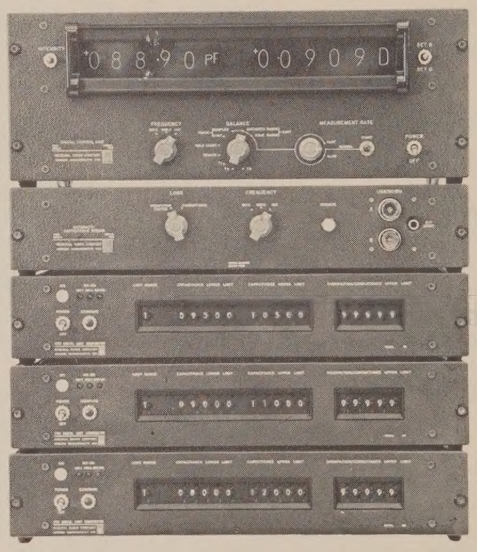
SINGLE-LIMIT CAPACITOR SORTING

For capacitor sorting, the comparator can be used with the Type 1680-A Automatic Capacitance Bridge Assembly. The bridge provides five-digit values of capacitance and dissipation factor or conductance with a basic accuracy of 0.1%. Measurements are made automatically at a rate of up to four per second.



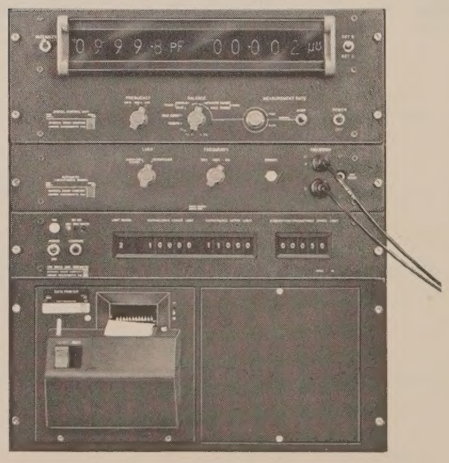
MULTIPLE-LIMIT SORTING

For multiple-limit sorting, up to ten comparators can be cascaded. With three comparators, as shown, capacitors can be sorted into four categories (for example, ±5%, ±10%, ±20%, and reject). The comparators provide visual go and no-go indications for manual sorting and control signals for automatic sorting.



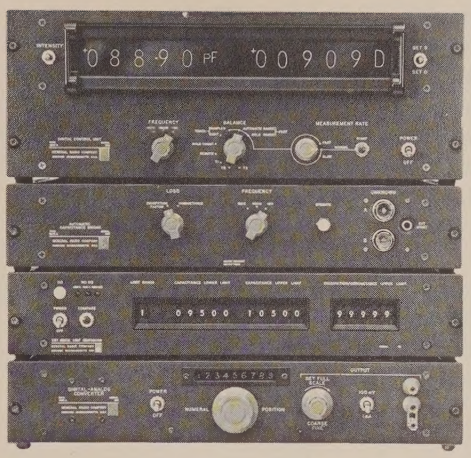
DIGITAL RECORDING

For digital recording of the measurement data, the comparator can be used with the Type 1137 Data Printer. The printer records up to twelve columns at a maximum rate of three lines per second. The comparator can be set so the printer records all measurement values, in-tolerance values only, or out-of-tolerance values only, and the printer can be set to print out-of-tolerance values in red.



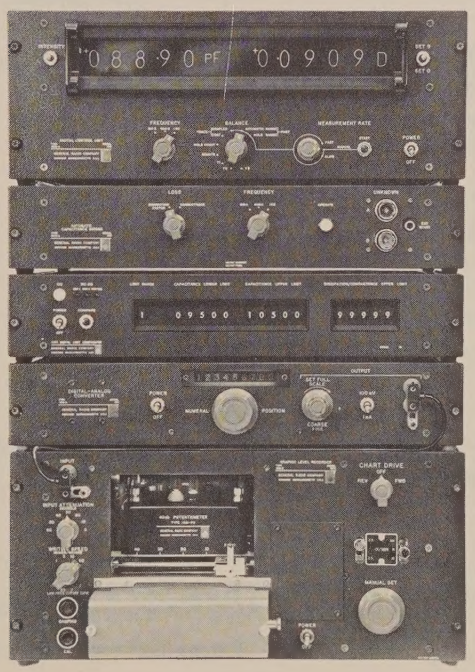
ANALOG OUTPUT AND X-Y RECORDING

For analog measurement data, the comparator can be used with the Type 1136 Digital-to-Analog Converter. The converter changes the digital data to voltage or current proportional to the numerical value. If an X-axis input is provided, an X-Y recorder can then be used to record capacitance vs temperature or capacitance vs voltage, etc.

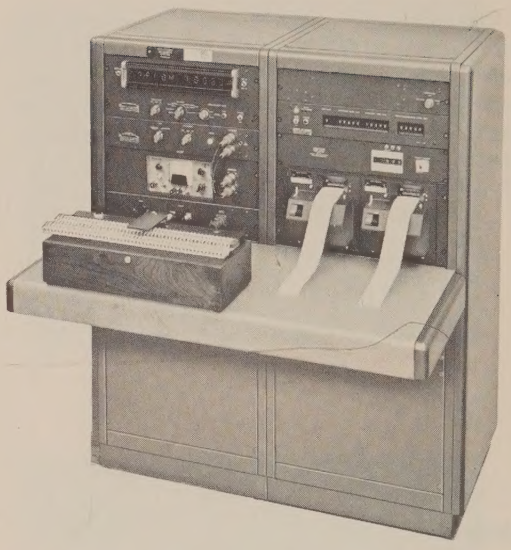


DC RECORDING

For dc records of the measurement data, the comparator can be used with the Type 1510 Digital-to-Graphic Recording Assembly. The assembly consists of a Type 1136 Digital-to-Analog Converter and a Type 1521 Graphic Level Recorder.



SYSTEMS



The Type 1781 Digital Limit Comparator and Type 1680-A Automatic Capacitance Bridge Assembly form a semi-automatic instrument assembly for the testing, sorting, or inspection of a variety of components. Since additional equipment will increase the processing speed and expand the capabilities of this basic assembly, General Radio has arranged to supply complete systems. Inquiries are invited.

Such systems are currently being used for laboratory development, production monitoring and final quality assurance, production-lot sorting, incoming inspection, environmental testing, and reliability evaluation.

Some of the measurements being made in these areas are:

Capacitance values and tolerances, dissipation factors, and temperature coefficients of thin-film, ceramic, polystyrene, paper, mica, glass, and metalized capacitors as well as solid, foil, thin-film, and polarized tantalum capacitors, electrolytics, variable-air capacitors, and capacitance decades.

Inductance of filter chokes.

Capacitance and impedance of multi-pair cables, multi-layer ceramic chips, and dielectric materials.

Resonance of L-C circuits.

Conductance of ionic solutions during reaction, conductance and capacitance of alkali-halide single crystals, permitivity and conductance of ferroelectric materials, and dielectric constant and dissipation factor of experimental polymers; all as a function of temperature.

And impedance of thin-oxide films on zirconium alloys as a function of time after immersion in various solutions.

Also see paragraph 2.14.

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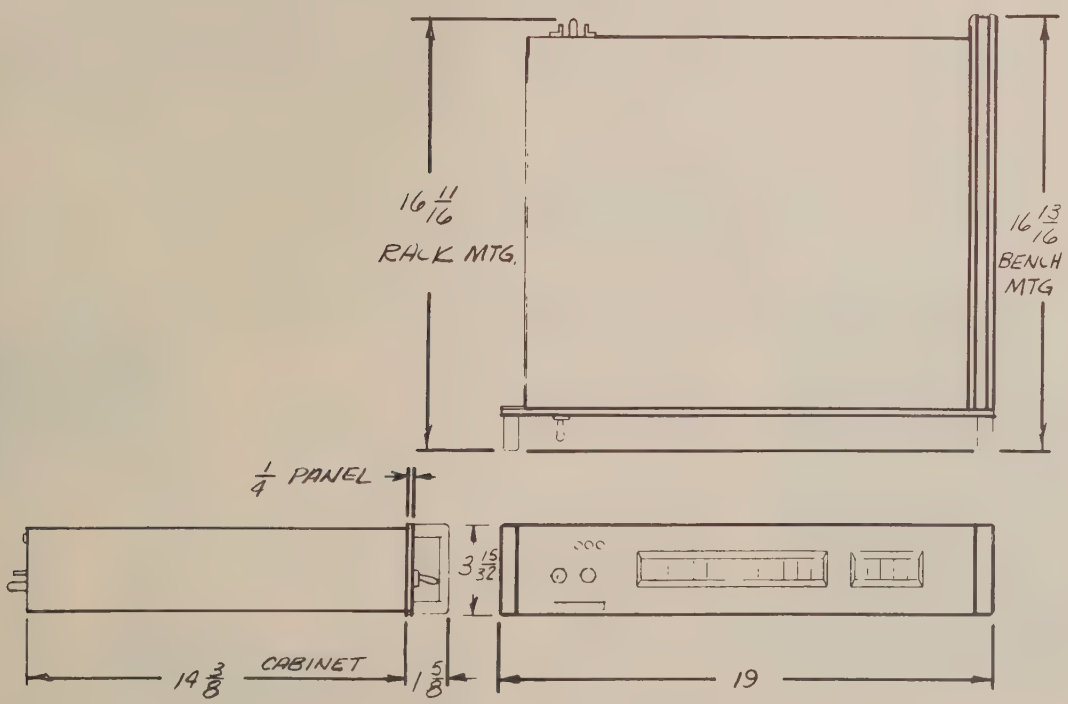
2.1 DIMENSIONS



2.2 ENVIROMENTAL

Ventilation. The instrument is convection cooled through vents on each side and should be mounted so that the vents are unobstructed.

Temperature. The instrument is designed to operate with ambient temperatures of 0 to 50 °C and is designed to be stored with ambient temperatures of -40 to +70 °C.

Humidity. The instrument is not affected by conditions of high humidity.

2.3 MOUNTING

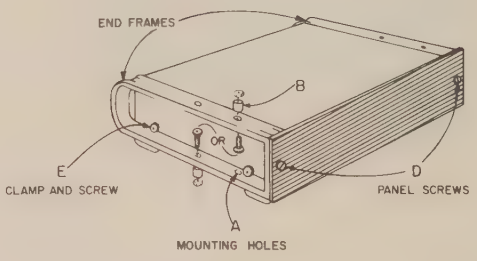
2.3.1 BENCH-RACK CONVERSION

The Type 1781 Digital Limit Comparator is supplied in two models, bench mount and rack mount. Either model may be converted to the other by the installation of a simple conversion set.

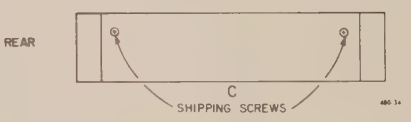
Model	*Use*	*Conversion Set*
Bench	For bench mounting and stack mounting	7863-9624 rack support set converts bench model to rack model
Rack	For rack mounting in a standard 19-inch relay rack	5310-9624 end-frame set converts rack model to bench model

2.3.2 BENCH MOUNTING (bench model)

The instrument normally rests on four rubber feet on top of a bench or shelf. However, holes (A) are provided in each end frame to allow permanent mounting on top or under a bench or shelf. Four 15/32-inch spacers (B) should be used for a more stable installation (part number 7660-2015 each).



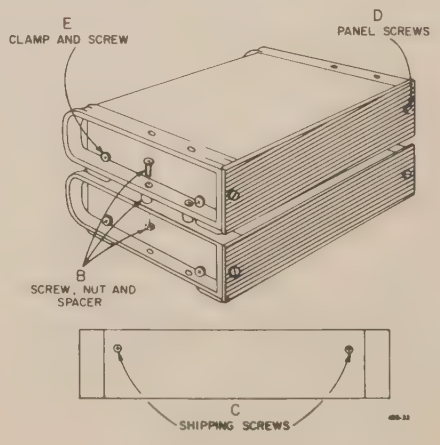
At the rear of the instrument, remove the two 10-32 binder-head shipping screws (C) that hold the cabinet to the chassis. These are used only for shipment and can be discarded.



This type of mounting permits either the chassis or the cabinet to be withdrawn independently. To remove the chassis and leave the cabinet mounted, loosen the panel screws (D) and slide the instrument forward out of the cabinet. To remove the cabinet and leave the chassis mounted, remove the eight clamps and screws (E) and pull the cabinet back off the chassis from the rear of the instrument.

2.3.3 STACK MOUNTING (bench model)

The instrument can be permanently assembled with another rack-bench instrument by bolting the end frames together with four 10-32 x 7/8 inch screws, four 10-32 nuts, and, for a more stable installation, four 5/32-inch spacers (B) (screws part number 7080-2900 each, nuts 5810-3300 each, spacers 7660-2015 each).



At the rear of the instrument, remove the two 10-32 binder-head shipping screws (C) that hold the cabinet to the chassis. These are used only for shipment and can be discarded.

This type of mounting permits the chassis of each instrument to be withdrawn independently. To remove the chassis, loosen the panel screws (D) and slide the instrument forward out of the cabinet.

2.3.4 RACK MOUNTING (rack model)

To install the instrument in a relay rack proceed as follows:

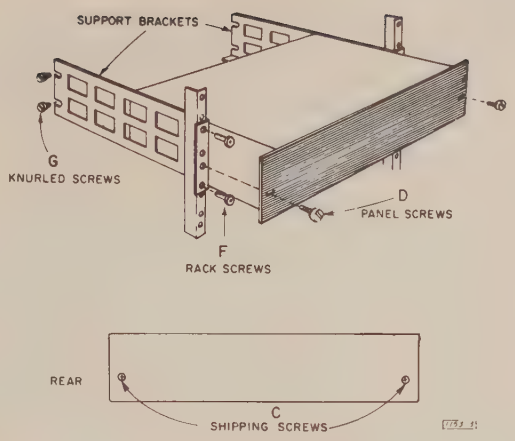
a. Attach each support bracket to the rack with two 10-32 binder-head screws (F). Use the outside holes on the brackets; face the bracket lips in.

b. Slide the instrument into the brackets as far as it will go.

c. Insert the panel screws (D) through the front panel and support brackets and screw them into the rack.

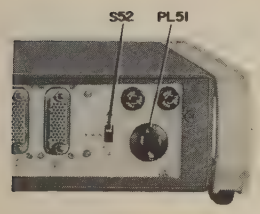
d. At the rear of the instrument, remove the two 10-32 binder-head shipping screws (C) that hold the cabinet to the chassis. These are used only for shipment and can be discarded.

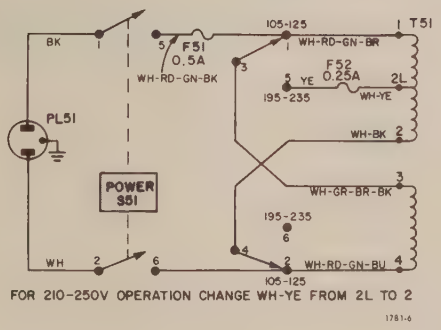
e. Insert the knurled screws (G) through the slots in the rear of the support brackets and screw them into the cabinet.

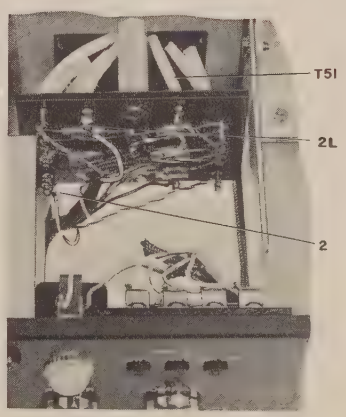


This type of mounting permits either the cabinet or the chassis to be withdrawn independently. To remove the chassis and leave the cabinet mounted, loosen the panel screws (D) and slide the instrument forward out of the cabinet. To remove the cabinet and leave the chassis mounted, remove the eight clamps and screws (E) and pull the cabinet back off the chassis from the rear of the instrument.

2.4 POWER CONNECTION







Power requirements are 105 to 125 volts, 195 to 235V, or 210 to 250 volts, 50 to 60 hertz, 10 watts. A line switch, S52, is provided on the rear of the instrument to convert from the 105- to 125-volt range to the 195-to-235-V range. Fuses remain the same for either range.

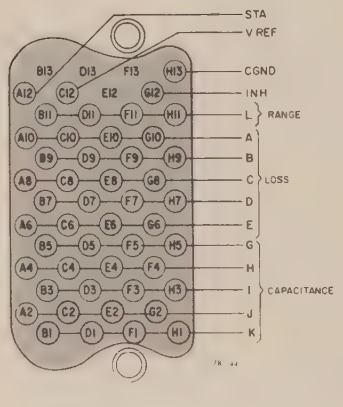
For the 210-to-250-V range, set the line switch to 195-235 and change the WH-YE lead on the power transformers, T51, from 2L to 2. Fuses remain the same.

Connection to the power line is made by means of a Type CAP-22 7-foot 3-wire power cord, supplied, which attaches to the power connector, PL51, on the rear of the instrument. The long cylindrical pin is connected directly to the metal case of the instrument (chassis ground, abbreviated CGND).

2.5 BCD DATA INPUT SOCKET, SO30

2.5.1 CONNECTIONS

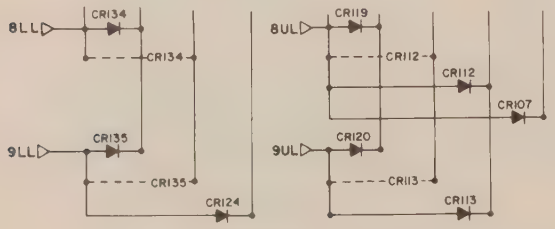
The data input signal is applied to the BCD DATA INPUT socket, SO30 on the rear of the instrument. This socket requires special tools for assembly and disassembly; see Section 6, parts list socket listing.



2.5.2 CHARACTERISTICS

	TYPE 1781 INPUT *BCD DATA INPUT, SO30*	TYPE 1680-A OUTPUT *DATA OUTPUT, SO3*
Digits	5 for capacitance 5 for loss 1 for range	5 for capacitance 5 for loss 1 for range
Code	BCD 1-2-4-2 (convertible to 1-2-4-8)	BCD 1-2-4-2 (1-2-4-8 available)
Logic levels	1 = 0 to 2V below reference 0 = 8 to 50V below reference Input impedance = 47kΩ Reference (VREF) must be within ±50V of chassis ground (CGND).	1 = reference (+6V) 0 = 12V below reference (-6V) Output impedance = 12kΩ Reference = +6V
Initiate	STA. Logic 1-0 transition. Minimum duration 2.5 ms. Input impedance 50kΩ.	PRT'. Logic 1-0 transition. Duration adjustable from 100 ms to ∞. Output impedance 10kΩ.

Code conversion. The instrument is normally wired for 1-2-4-2 BCD but can be easily converted to 1-2-4-8 by changes in the connections of four diodes (CR112, 113, 134, and 135) on the format board. The true function is the logic-1 level which is always positive with respect to the logic-0 level.



FORMAT BOARD (H)
DOTTED LINES SHOW CONNECTIONS FOR 1-2-4-8 WEIGHTED BCD

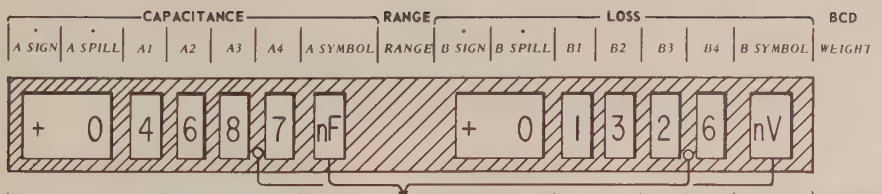
DECIMAL	1-2-4-2 BCD	1-2-4-8 BCD
0	0000	0000
1	1000	1000
2	0100	0100
3	1100	1100
4	0010	0010
5	1010	1010
6	0110	0110
7	1110	1110
8	0111	0001
9	1111	1001

Logic-level explanation. In order to accommodate a large variety of input signals, all circuits in the instrument are referenced to a floating ground potential (VREF).

This potential is ordinarily determined by the data input source and must be within ±50V of chassis ground; source resistance must be 1kΩ or less.

Connection to VREF is pin C12 of the rear-mounted sockets and is +6V (with reference to chassis ground) from the Type 1680-A.

2.5.3 DATA SIGNALS

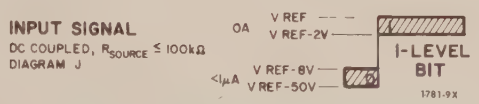


1680-A SIGNAL (SO3)		SPOA	E1A1	E1A2	E1A3	E1A4		E1R		SPOB	E1B1	E1B2	E1B3	E1B4		
PIN		B1	A2	B3	A4	B5		B11		A6	B7	A8	B9	A10		1
1781 SIGNAL (SO30)		**K1**	**J1**	**I1**	**H1**	**G1**		**L1**		**E1**	**D1**	**C1**	**B1**	**A1**		
1680-A SIGNAL (SO3)		PA	F1A1	F1A2	F1A3	F1A4		F1R		PB	F1B1	F1B2	F1B3	F1B4		
PIN		D1	C2	D3	C4	D5		D11		C6	D7	C8	D9	C10		2
1781 SIGNAL (SO30)		**K2**	**J2**	**I2**	**H2**	**G2**		**L2**		**E2**	**D2**	**C2**	**B2**	**A2**		
1680-A SIGNAL (SO3)		PTR	G1A1	G1A2	G1A3	G1A4		G1R		PTR	G1B1	G1B2	G1B3	G1B4		
PIN		F1	E2	F3	E4	F5		F11		E6	F7	E8	F9	E10		4
1781 SIGNAL (SO30)		**K3**	**J3**	**I3**	**H3**	**G3**		**L3**		**E3**	**D3**	**C3**	**B3**	**A3**		
1680-A SIGNAL (SO3)		PTR	H1A1	H1A2	H1A3	H1A4		H1R		PTR	H1B1	H1B2	H1B3	H1B4		
PIN		H1	G2	H3	G4	H5		H11		G6	H7	G8	H9	G10		2'
1781 SIGNAL (SO30)		**K4**	**J4**	**I4**	**H4**	**G4**		**L4**		**E4**	**D4**	**C4**	**B4**	**A4**		

* Sign and spill information is combined in a single 4-bit BCD output. The **PTR** signal from the Type 1680-A is a 0-level (-9V) signal whose only function is to complete the sign-spill binary code.

SIGN	SPILL	BCD	DECIMAL
+	0	0000	0
+	1	1000	1
−	0	0100	2
−	1	1100	3

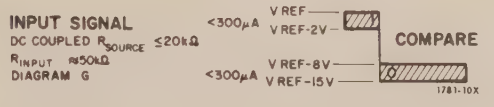
A1 through L4. The data input signals are applied to inputs A1 through L4. The signals must remain at least 2.5 ms to allow the Type 1781 time to complete the comparison.



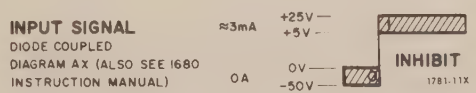
2.5.4 CONTROL SIGNALS

1680-A SIGNAL (SO3)	PRT′	IXP	+6V	GND
PIN	A12	G12	C12	H13
1781-A SIGNAL (SO30)	**STA**	**INH**	**VREF**	**CGND**

STA, compare initiate. The comparator requires a signal to start the comparison. The start signal must be a 1-0 transition from the input source (PRT′ signal from the Type 1680-A) applied to the STA input of the comparator (pin A12 of the BCD DATA INPUT connector). The signal must remain at the 0-level at least 2.5 ms to allow the Type 1781 time to complete the comparison.



INH, balance inhibit. A 1-level INH signal applied to the Type 1680-A (IXP input, pin G12 of the DATA OUTPUT connector) prevents the bridge from starting a balance operation or stops the balance operation if one is already in progress. It does not prevent or stop presetting (setting the registers to 02000 before the start of a balance) but it can be used to delay the start of the actual balance operation until the external circuit is ready. The INH signal originates in the external source and indicates the source is busy; e.g., if the source is a printer, it indicates the printer is setting up for a print operation, printing, or recovering from a print operation and is not ready to receive new data. The comparator acts only as a junction point for the inhibit signal which is applied to pin G12 of the BCD DATA OUTPUT socket, SO32, passes directly to pin G12 of the BCD DATA INPUT socket SO30, and then is applied to pin G12 of the Type 1680-A DATA OUTPUT socket SO3. For further details, see paragraph 2.11.



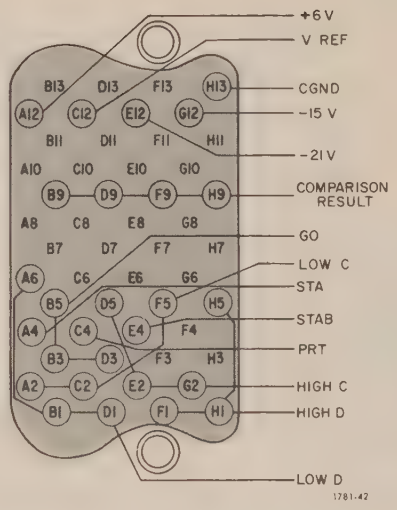
VREF, floating ground. See Logic Levels, opposite page.

CGND, chassis ground. Chassis ground.

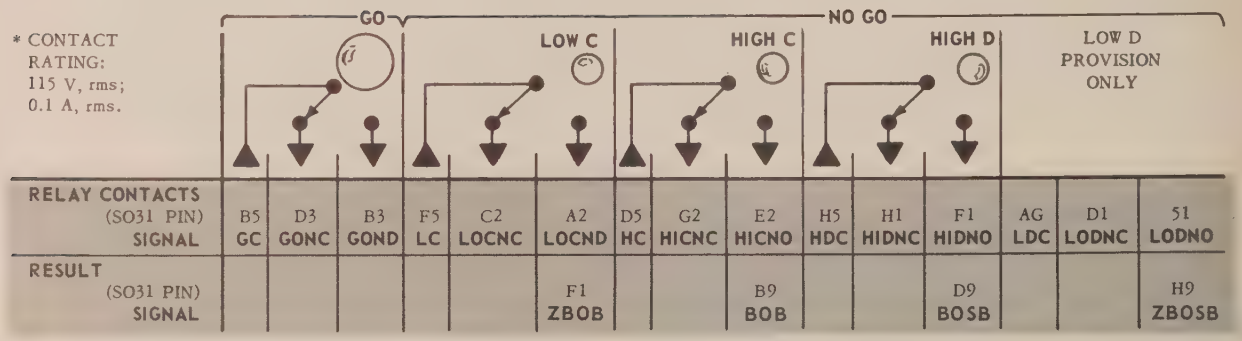
2.6 RELAY CONTACTS OUTPUT SOCKET, SO31

2.6.1 CONNECTIONS

The RELAY CONTACTS socket, SO31 on the rear of the instrument, provides connections to the contacts of four spdt relays that can be used to drive external equipment such as component sorting devices. This socket requires special tools for assembly and disassembly; see Section 6, parts list socket listing.

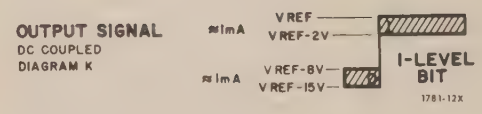


2.6.2 DATA SIGNALS



RELAY CONTACTS (SO31 PIN)	B5	D3	B3	F5	C2	A2	D5	G2	E2	H5	H1	F1	AG	D1	51
SIGNAL	GC	GONC	GOND	LC	LOCNC	LOCND	HC	HICNC	HICNO	HDC	HIDNC	HIDNO	LDC	LODNC	LODNO
RESULT (SO31 PIN)						F1			B9			D9			H9
SIGNAL						ZBOB			BOB			BOSB			ZBOSB

Comparison result. In addition to relay-contact connections, the instrument also provides BCD signals (ZBOB, BOB, BOSB, and ZBOSB) to indicate the results of the comparison. For BCD-code and logic-level information, see paragraph 2.5.2.



INDICATION	LOW C	HIGH C	HIGH D	LOW D	DECIMAL
GO	0	0	0	0	0
LOW C	1	0	0	0	1
HIGH C	0	1	0	0	2
HIGH D	0	0	1	0	4
LOW C, HIGH D	1	0	1	0	5
HIGH C, HIGH D	0	1	1	0	6

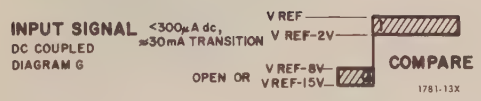
**Rating is with contact-protection values of 0.0047μF and 120Ω. With changes in these values, relays can be protected from highly inductive loads or can be protected up to 100 VA (2A max, 500V max); write factory for specific details on individual requirements.*

2.6.3 CONTROL SIGNALS

SO31 PIN	A4	E4	C4	A12	G12	E12	C12	H13
SIGNAL	**STA**	**STAB**	**PRT**	**+6V**	**-15V**	**-21V**	**VREF**	**CGND**

STA, compare initiate. See paragraph 2.5.4.

STAB. Ordinarily, a comparison is initiated by the STA signal (PRT from the Type 1680-A which occurs after each balance operation) and after each comparison a PRT′ signal is issued from the comparator to trigger peripheral equipment such as a printer.



Often it is desirable to initiate several comparisons on a single measurement value from the Type 1680-A or other input source (to check the comparator limit settings, for example) or to initiate comparisons but not PRT signals (to prevent triggering peripheral equipment while the comparator limits are being checked).

The STAB signal provides this capability; it initiates comparisons but does not allow the comparator to issue PRT signals. The STAB signal ordinarily comes from the COMPARE button, S904 on the front panel, but may originate remotely.

PRT, print command. See paragraph 2.7.4.

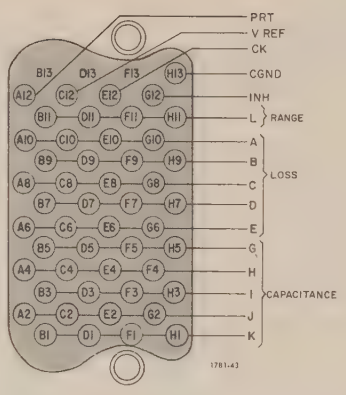
VREF, floating ground. See paragraph 2.5.2.

CGND, chassis ground. Chassis ground.

2.7 BCD DATA OUTPUT SOCKET, SO32

2.7.1 CONNECTIONS

Measurement data is available at the BCD DATA OUTPUT socket, SO32 on the rear of the instrument, for use by a printer, recorder, digital-to-analog converter, another comparator, or other data processing equipment. This socket requires special tools for assembly and disassembly; see Section 6, parts list socket listing.



2.7.2 CHARACTERISTICS

Same as for the BCD DATA INPUT socket SO30; see paragraph 2.5.2.

2.7.3 DATA SIGNALS

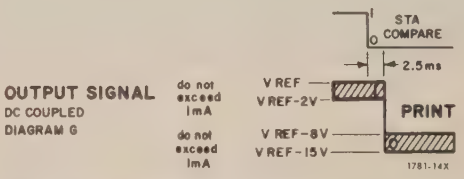
Same as for the BCD DATA INPUT socket SO30 (the data signals to the two sockets are wired in parallel); see paragraph 2.5.3.

2.7.4 CONTROL SIGNALS

SO32 PIN	A12	E12	G12	C12	H13
SIGNAL	PRT	CK	INH	VREF	CGND

The control-signal connections to the BCD DATA OUTPUT socket are the same as the control-signal connections to the BCD DATA INPUT socket (paragraph 2.5.4) except the PRT signal replaces the STA signal and a CK signal has been added.

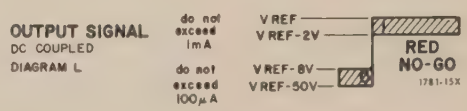
PRT, print command. Most auxiliary equipment requires a start signal to initiate the operation. The start signal from the comparator is the PRT signal which is a 1-0 transition that occurs after the Type 1781 has completed a comparison. Its characteristics are identical to those of the STA signal to the comparator (paragraph 2.5.4; i.e., the PRT′ signal from the Type 1680-A) except it is delayed 2.5 ms to allow time for the comparison and it is gated by the DATA READY COMMAND CONTROL, S903 on the rear of the comparator.



DATA READY COMMAND CONTROL. The DATA READY COMMAND CONTROL, a screwdriver-operated switch S903 on the rear of the instrument gates the PRT print command signal as follows:

1. PRINT ALL – – – – – – – – – – – – – – – – – PRT signal occurs after each comparison.
2. PRINT IN-TOLERANCE ONLY – – – – – – PRT signal occurs only if comparison resulted in a GO indication.
3. PRINT OUT-OF-TOLERANCE ONLY – – – PRT signal occurs only if comparison resulted in a NO-GO indication.

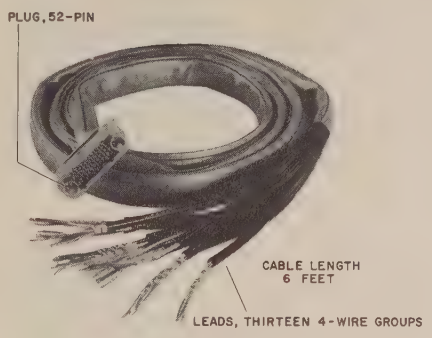
CK, color command. When the comparator is used with a Type 1137 Data Printer and the RED/BLACK switch on the printer is set to RED, a 0-level CK signal (GO or in-tolerance indication) sets the printer for a black print-out and a 1-level CK signal (NO-GO or out-of-tolerance indication) sets the printer for a red print-out.



2.8 CABLE ASSEMBLIES

2.8.1 4205-1010 UNIVERSAL CABLE, ONE CONNECTOR

The 4205-1010 cable is primarily intended to connect non-GR instruments to the sockets on the rear of the comparator. The plug requires special tools for assembly; see Section 6, parts list socket listing.

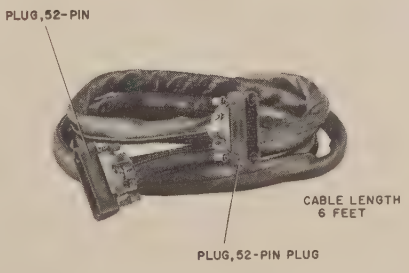


Connections:

PLUG PIN	LEAD GROUP	LEAD COLOR	PLUG PIN	LEAD GROUP	LEAD COLOR	PLUG PIN	LEAD GROUP	LEAD COLOR	PLUG PIN	LEAD GROUP	LEAD COLOR
B1	1	brown	A4	4	brown	B7	7	brown	A10	10	brown
D1		red	C4		red	D7		red	C10		red
F1		orange	E4		orange	F7		orange	E10		orange
H1		yellow	G4		yellow	H7		yellow	G10		yellow
A2	2	brown	B5	5	brown	A8	8	brown	B11	11	brown
C2		red	D5		red	C8		red	D11		red
E2		orange	F5		orange	E8		orange	F11		orange
G2		yellow	H5		yellow	G8		yellow	H11		yellow
B3	3	brown	A6	6	brown	B9	9	brown	A12	12	brown
D3		red	C6		red	D9		red	C12		red
F3		orange	E6		orange	F9		orange	E12		orange
H3		yellow	G6		yellow	H9		yellow	G12		yellow
									H13	C	black
									B13		green
									D13		blue
									F13		white

2.8.2 4205-1000 UNIVERSAL CABLE, TWO CONNECTORS

The 4205-1000 Cable is identical to the 4205-1010 cable above, except both ends are terminated in 52-pin plugs. The plugs require special tools for assembly and disassembly; see Section 6, parts list socket listing.



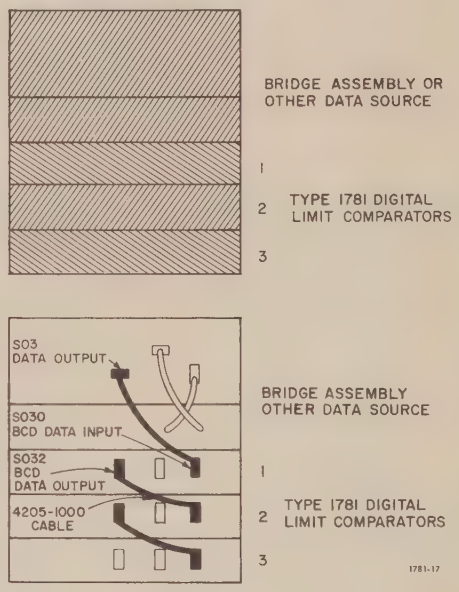
2.9 LIMIT SORTING

A single comparator can be used with an input source such as the Type 1680-A Automatic Capacitance Bridge Assembly for single-limit testing or up to ten can be used for multiple-limit testing.

If a single comparator is used, its rear-mounted DATA READY COMMAND CONTROL can be set to any desired position (for a description of this control, see paragraph 2.7.4).

If several comparators are used, their rear-mounted DATA READY COMMAND CONTROLS must be set to PRINT OUT-OF-TOLERANCE ONLY (except the last which can be set to any desired position) and the LIMIT switches must be set so that the limits of the first comparator are the narrowest and the limits of the last comparator are the broadest. For example, a group of nominal 1-μF capacitors are to be sorted into four categories, ±5%, ±10%, ±20%, and reject:

COMP	UNK TOL	DATA READY COM CON	RANGE	LOWER LIMIT	UPPER LIMIT
1	± 5%	PRINT OUT OF TOLERANCE ONLY	5	09500	10500
2	±10%	PRINT OUT OF TOLERANCE ONLY	5	09000	11000
3	±20%	———	5	08000	12000



CONNECTIONS TO SORTING EQUIPMENT

Connections to sorting equipment are made to the RELAY CONTACTS OUTPUT socket, SO31 on the rear of the instrument (more fully described in paragraph 2.6). A 4205-1010 universal cable (paragraph 2.8.1) may be used.

Multiple-group sorting. A single comparator can sort components into six groups:

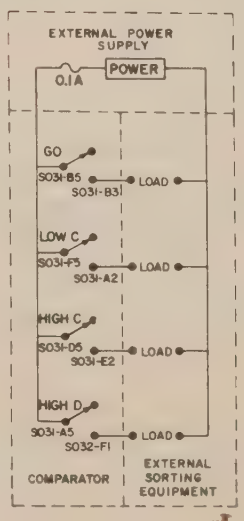
1. GO — in tolerance
2. LOW C — capacitance below limit
3. HIGH C — capacitance above limit
4. HIGH D/G — loss above limit
5. LOW C and HIGH D/G — capacitance below limit and loss above limit
6. HIGH C and HIGH D/G — capacitance above limit and loss above limit

Multiple-limit sorting. Several comparators can sort components into multiple-limit categories. For example, three comparators can sort components into four categories:

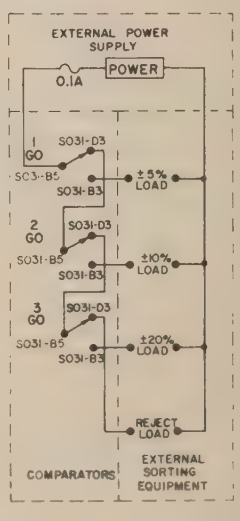
1. ±5%
2. ±10%
3. ±20%
4. Reject

} or any other tolerances

MULTIPLE-GROUP



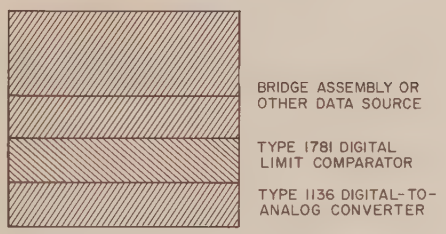
MULTIPLE-LIMIT

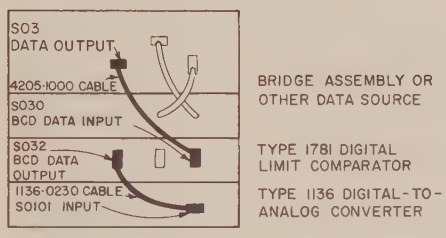


2.10 ANALOG OUTPUT

A digital-to-analog converter can be used to convert the digital measurement data from the comparator to analog information. An analog output is useful to automatically plot capacitance vs temperature, capacitance vs bias voltage, or dissipation factor vs temperature, etc. The Type 1136 Digital-to-Analog Converter will select any three consecutive columns, or the last two columns, from the comparator and convert them to a voltage or current proportional to the numerical value.

The converter connects to the BCD DATA OUTPUT socket, SO32 on the rear of the comparator, which is described in paragraph 2.7.





EQUIPMENT

1136-9402 Bench model Type 1136 Digital-to-Analog Converter for use with the comparator. Includes 1136-0230 cable.

1136-9502 Rack model Type 1136 Digital-to-Analog Converter for use with the comparator. Includes 1136-0230 cable.

1136-0230 Single converter cable; supplied with 1136-9402 and 1136-9502 converters.

1136-0270 Double converter cable; available to connect two converters to comparator.

OUTPUT

The 1136-0230 cable is wired so that capacitance data from the bridge is connected to digits 1 through 5 in the converter, nothing is connected to digit 6, and the last three loss figures are connected to digits 7 through 9. Other formats are possible with changes in the cable wiring.

Simultaneous analog outputs of both capacitance and loss requires two converters and an 1136-0270 double converter cable.

The full scale output (999 level) is adjustable by means of two front-panel controls.

CONVERTER SOURCE IMPEDANCE	BINARY INPUT	CONVERTER VOLTAGE	OUTPUT CURRENT
15 kΩ	000	0	0
	999	15 V	1 mA
100 Ω	000	0	0
	999	100 mA	1 mA

1680-A VISUAL REGISTER

OUTPUT

CONVERTER DIGITS

1	2	3	4	5	6	7	8	9
1	4	6						
		or						
	4	6	8					
			or					
		6	8	7				
	-			or				
			8	7				
					or			
						3	2	6
								or
							2	6	0

2.11 DIGITAL RECORDING

A digital printer can be used to record the measurement data. The Type 1137 Data Printer records up to twelve columns at a maximum print rate of three lines per second. The DATA READY COMMAND CONTROL, S904 on the rear of the comparator, can be set so the printer records all measurement values, in-tolerance values only, or out-of-tolerance values only. The printer can be set to print out-of-tolerance values in red.

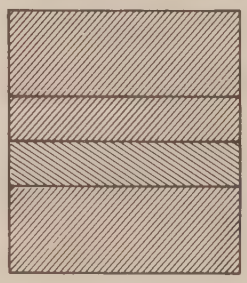
EQUIPMENT

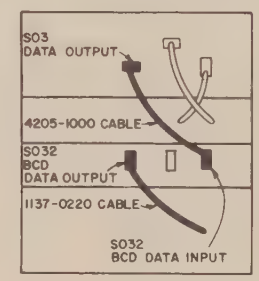
1137-9743 Portable model Type 1137 Data Printer for use with the comparator. Includes six BCD Plug-In Code Modules for 6-column print out and an 1137-0220 cable which can handle up to 11 columns.

1137-9744 Rack model Type 1137 Data Printer for use with the comparator. Includes six BCD Plug-In Code Modules for 6-column print out and an 1137-0220 cable which can handle up to 11 columns.

1137-0220 11-column cable; supplied with 1137-9743 and 1137-9744 printers.

1137-9604 BCD Plug-In Code Modules; available to increase printer capacity up to a maximum of 12 columns.





RECORD

A, 6 column. Standard 1137-9743 or 1137-9744 printer. Columns 1 through 5 indicate capacitance and column 12 indicates range.

B, 11 column. 1137-9747 or 1137-9744 with 5 additional 1137-9064 modules. Columns 1 through 5 indicate capacitance, columns 7 through 11 indicate loss, and column 12 indicates range.

C, 11 column. Same as above except first digit of loss was dropped (it is usually zero when capacitors are measured) to provide a space between loss and range.

Digits can be arranged in any order by interchanging the socket for each digit. This is done inside the printer where the modules plug into the cable connectors. A table on the rear of the printer shows which socket is associated with each column of the printer.

1680-A VISUAL REGISTER

PRINT OUT

PRINTER COLUMNS

	1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*
A	1	4	6	8	7							2
B	1	4	6	8	7		0	1	3	2	6	2
C	1	4	6	8	7		1	3	2	6		2

CONTROL SIGNALS

In addition to the measurement data BCD signals, the printer requires a signal to initiate the print operation. For the Type 1137 Data Printer, this signal must be a 1-0 transition, must remain 0 for at least 100 ms to allow the printer to set-up and print, and must return to 1 at least 15 ms before the next print command to allow the printer to recover.

PRT, print command. The 1-0 transition of the PRT signal from the comparator is the print command signal to the printer. The 0-level of the PRT signal indicates the Type 1781 has completed a comparison and the measurement data is ready to be used.

INH, balance inhibit. The INH input from the printer to the comparator (which passes directly to the bridge assembly) prevents the Type 1680 Automatic Capacitance Bridge Assembly from starting a new balance operation while the printer is setting up for a print operation, printing, or recovering from a print operation.

The INH signal does not prevent the bridge from presetting and therefore is not normally used with the Type 1680. Instead, the MEASUREMENT RATE control on the bridge assembly is set so the maximum print rate of the printer is not exceeded. This ensures the print command is issued at a time when both the printer and the bridge are ready.

CK, color command. If the RED/BLACK switch on the printer is set to RED, a 0-level CK signal (GO or in-tolerance indication) from the comparator sets the printer for a black print-out and a 1-level CK signal (NO-GO or out-of-tolerance indication) sets the printer for a red print-out.

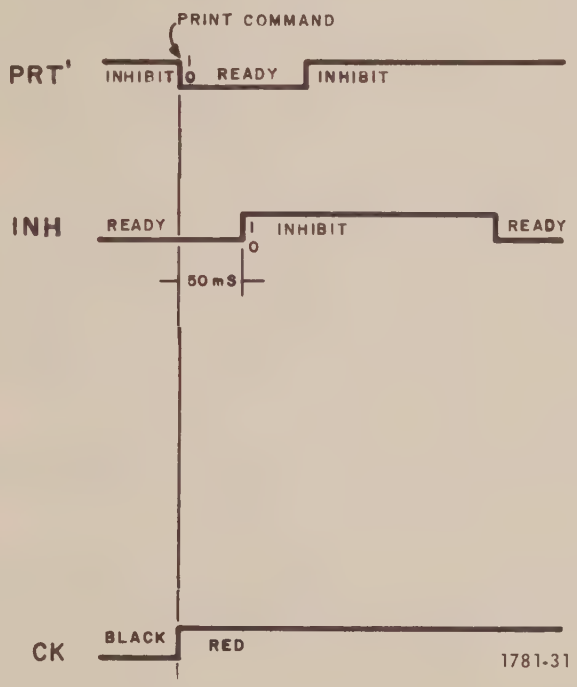
MANUAL PRINT

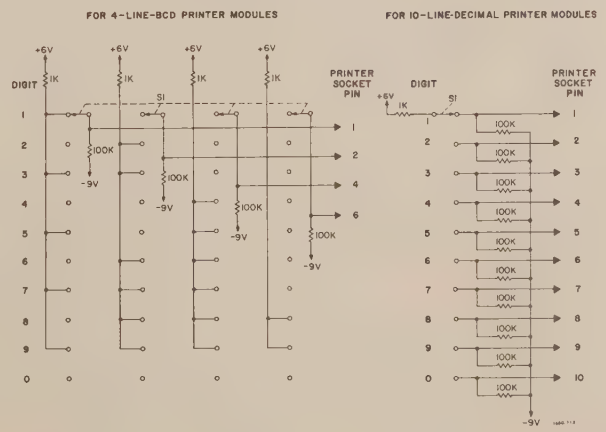
Serial-number information (or any other numerical data) can be manually inserted in the printer by means of an external switch box. The circuit configuration of the box depends on the type of code modules used in the printer (1137-9604 BCD or 1137-9605 Decimal). One switch for each digit is necessary; e.g., if the highest number is 999, three switches are required.

In addition to the wiring shown, a print command is necessary (see PRT above).

Also, to prevent the recording of false data, the print command must be given when the bridge assembly or other data source is ready; i.e., not presetting, balancing, or otherwise changing data.

The printer connects to the BCD DATA OUTPUT socket, SO32 on the rear of the comparator, which is described in paragraph 2.7.





2.12 DC RECORDING

If the digital output of the bridge has been converted to an analog output (paragraph 2.10), a dc level recorder can be used to record the data. This is useful for permanent records of the value of different capacitors or of the capacitance changes vs time, etc.

EQUIPMENT

1521-9802 Bench model Type 1521 Graphic Level Recorder. Does *not* include necessary 1521-3007 dc potentiometer or 0247-9892 patch cord.

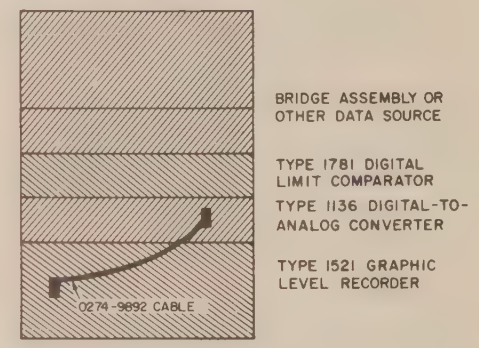
1521-9812 Rack model Type 1521 Graphic Level Recorder. Does *not* include necessary 1521-3007 dc potentiometer or 0274-9892 patch cord.

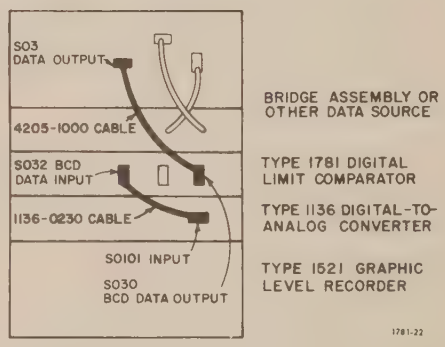
1510-9402 Type 1510 Digital-to-Graphic Recording Assembly for either bench or rack mount. Includes Type 1136 Digital-to-Analog Converter, Type 1521 Graphic Level Recorder, 1521-3007 dc potentiometer, 0274-9892 patch cord, and 1136-0230 single converter cable.

1521-3007 Dc potentiometer. Necessary to adapt Type 1521 for use with Type 1136. Supplied with 1510-9402 recording assembly.

0274-9892 Type 274-NPM Double-Plug Patch Cord; double 3/4-inch-spaced banana plugs on each end. For connection from converter to recorder. Supplied with 1510-9402 recording assembly.

1136-0230 Single converter cable; supplied with 1510-9402 recording assembly.


BRIDGE ASSEMBLY OR OTHER DATA SOURCE
TYPE 1781 DIGITAL LIMIT COMPARATOR
TYPE 1136 DIGITAL-TO-ANALOG CONVERTER
TYPE 1521 GRAPHIC LEVEL RECORDER
0274-9892 CABLE



RECORD

The Type 1521 or 1510 provides a 4-inch recording with a speed of 2.5, 7.5, 25, and 75 inches per minute or (with optional motors) of 0.5, 1.5, 5, and 7.5 inches per minute or 2.5, 7.5, 25, and 75 inches per hour.

2.13 X-Y RECORDING

If the digital output of the comparator has been converted to an analog output and if an X-axis input is provided, an X-Y recorder can be used to record the data. This is useful for plots of capacitance vs temperature, or capacitance vs voltage, etc.

EQUIPMENT

The following companies make X-Y recorders compatible with the output of the Type 1136 Digital-to-Analog Converter:

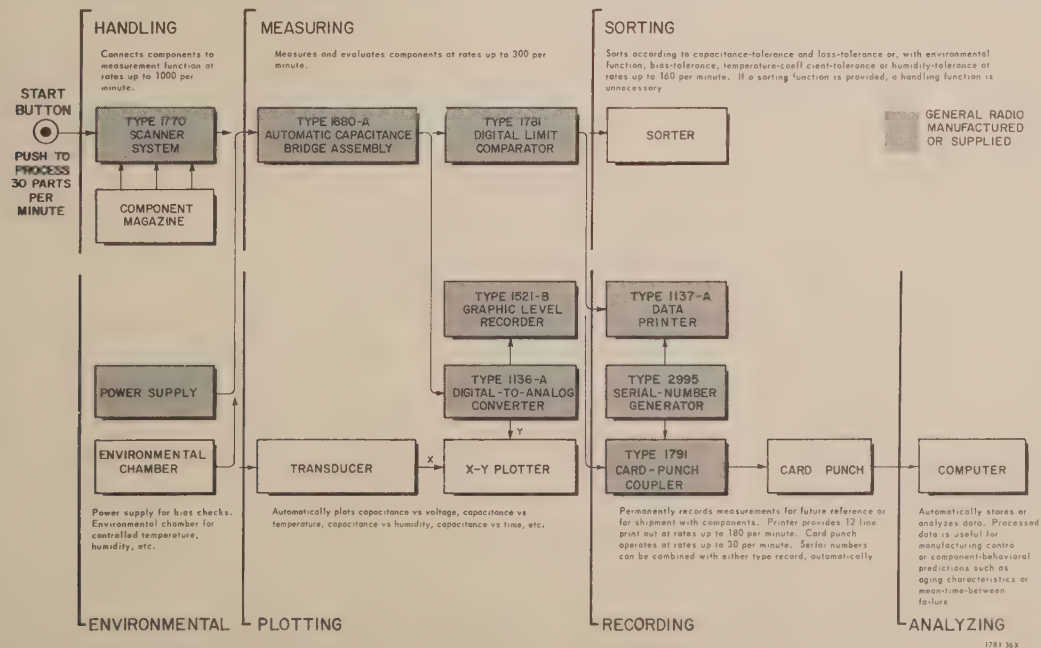
Electro Instrument Incorporated, 8611 Balboa Avenue, San Diego, California
Electronic Associates Incorporated, West Long Beach, New Jersey
F.L. Mosley Company, Pasadena, California
Houston Instrument Corporation, 4950 Terminal Avenue, Bellaire, Texas
Leeds and Northrup Company, 4901 Stantor Avenue, Philadelphia, Pennsylvania
Sanborn Company, 175 Wyman Street, Waltham, Massachusetts
Varian Associates, 611 Hansen Way, Palo Alto, California

The following companies make transducers to convert temperature to voltage (for the X-axis input):

Lion Research Corporation, 32 Potter Street, Cambridge, Massachusetts 02141
Disa Electronik A/S, Herley, Denmark.

2.14 SYSTEMS

The comparator and its companion instrument, the automatic bridge, form the nucleus of a larger system designed to solve specific measurement problems. Each system is custom tailored to individual requirements by General Radio and includes only the equipment necessary to perform the required task; completely assembled and checked as a unit.


HANDLING
Connects components to measurement function at rates up to 1000 per minute.
MEASURING
Measures and evaluates components at rates up to 300 per minute.
SORTING
Sorts according to capacitance-tolerance and loss-tolerance or, with environmental function, bias-tolerance, temperature-coeff cient-tolerance or humidity-tolerance at rates up to 160 per minute. If a sorting function is provided, a handling function is unnecessary
START BUTTON
PUSH TO PROCESS 30 PARTS PER MINUTE
TYPE 1770 SCANNER SYSTEM
COMPONENT MAGAZINE
TYPE 1680-A AUTOMATIC CAPACITANCE BRIDGE ASSEMBLY
TYPE 1781 DIGITAL LIMIT COMPARATOR
SORTER
GENERAL RADIO MANUFACTURED OR SUPPLIED
TYPE 1521-B GRAPHIC LEVEL RECORDER
TYPE 1137-A DATA PRINTER
TYPE 1136-A DIGITAL-TO-ANALOG CONVERTER
TYPE 2995 SERIAL-NUMBER GENERATOR
POWER SUPPLY
ENVIRONMENTAL CHAMBER
TRANSDUCER
X
Y
X-Y PLOTTER
TYPE 1791 CARD-PUNCH COUPLER
CARD PUNCH
COMPUTER
Power supply for bias checks. Environmental chamber for controlled temperature, humidity, etc.
Automatically plots capacitance vs voltage, capacitance vs temperature, capacitance vs humidity, capacitance vs time, etc.
Permanently records measurements for future reference or for shipment with components. Printer provides 12 line print out at rates up to 180 per minute. Card punch operates at rates up to 30 per minute. Serial numbers can be combined with either type record, automatically
Automatically stores or analyzes data. Processed data is useful for manufacturing contro or component-behavioral predictions such as aging characteristics or mean-time-between failure
ENVIRONMENTAL
PLOTTING
RECORDING
ANALYZING
1781 36x

3.1 Preliminary - - - - - - - - - - - - - - - - - - - 3-1
3.2 Operation - - - - - - - - - - - - - - - - - - - 3-3

3.1 PRELIMINARY

3.1.1 CONNECTIONS (more fully described in Section 2 Installation)

Data source. Connect the BCD DATA INPUT socket of the comparator to the input data source (to the DATA OUTPUT socket of the Type 1680-A Automatic Capacitance Bridge Assembly).

Sorting equipment. Connect the RELAY CONTACTS OUTPUT socket of the comparator to the sorting equipment, if used.

Supplementary equipment. Connect the BCD DATA OUTPUT socket of the comparator to any supplementary equipment, such as a printer, recorder, digital-to-analog converter, another comparator, or other data processing equipment.

Power. Connect the comparator to the power line.

CAUTION

Be sure the line switch on the rear of the instrument is set for the proper line voltage.

3.1.2 OPERATIONAL CHECKS

Data source. Set the controls as necessary on the input data source for a fixed measurement value. If the source is a Type 1680-A, set the controls as follows:

FREQUENCY – – – – – – – – – – – – – – – – both at 1 KC
BALANCE – – – – – – – – – – – – AUTOMATIC RANGE
MEASUREMENT RATE – – – – – – – – – – – – MANUAL
LOSS – – – – – – – – – – – – – – – DISSIPATION FACTOR

Comparator. Set the controls as follows:
LIMIT RANGE – – – – – – – – same range as data source
for 1680-A: 000.00**pF** = range 1, 0000.0**nF** = range 5
0000.0**pF** = range 2, 00.000μ**F** = range 6
00.000**nF** = range 3, 000.00μ**F** = range 7
000.00**nF** = range 4
CAPACITANCE LOWER LIMIT – – – – – – – – – – 00000
CAPACITANCE UPPER LIMIT – – – – – – – – – – 99999
DISSIPATION/CONDUCTANCE UPPER LIMIT – – 99999

PROCEDURE

AA Connect an unknown of from 200pF to 1 μF and push the START button to obtain a balance.

A Push COMPARE button; GO lamp should light.

B Set LIMIT RANGE switch up one digit from proper range and push COMPARE button; LOW C lamp should light.

C Set LIMIT RANGE switch down one digit from proper range and push COMPARE button; HIGH C lamp should light.

D Set LIMIT RANGE switch to proper range and push COMPARE button; GO lamp should light.

E Set CAPACITANCE LOWER LIMIT switches one digit above proper value and push COMPARE button; LOW C lamp should light.

F Set CAPACITANCE LOWER LIMIT switches to proper value and push COMPARE button; GO lamp should light.

G Set CAPACITANCE UPPER LIMIT switches one digit below proper value and push COMPARE button; HIGH C lamp should light.

H Set CAPACITANCE UPPER LIMIT switches to proper value and push COMPARE button; GO lamp should light.

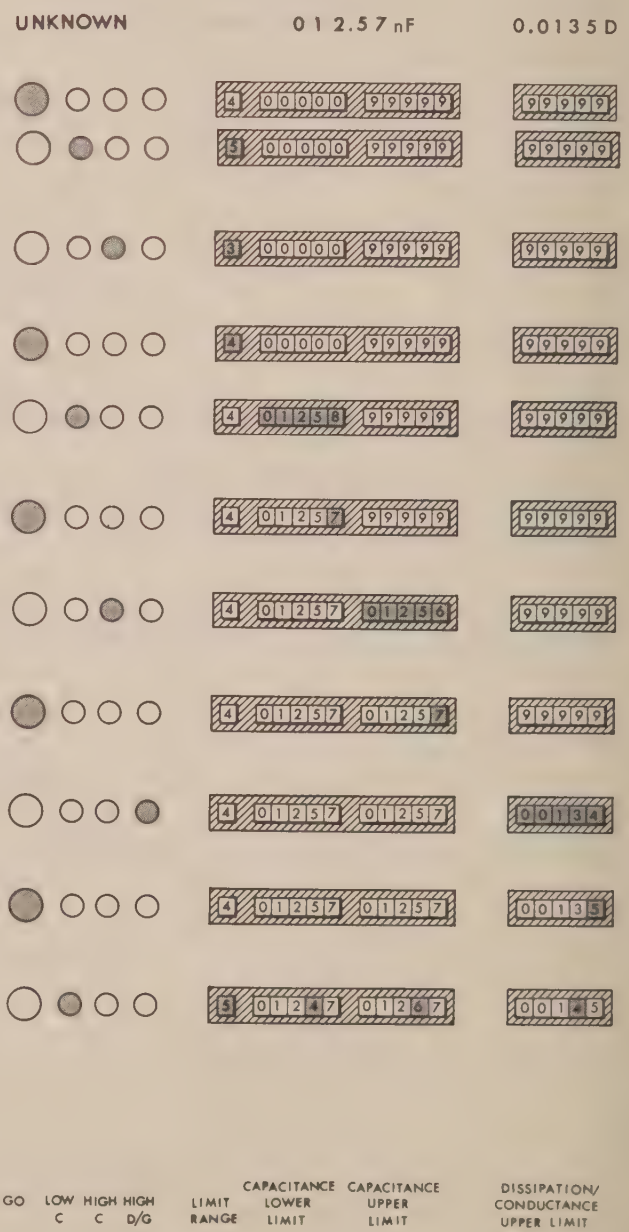
I Set DISSIPATION/CONDUCTANCE UPPER LIMIT switches one digit below proper value and push COMPARE button; HIGH D/G lamp should light.

J Set DISSIPATION/CONDUCTANCE UPPER LIMIT switches to proper value and push COMPARE button; GO lamp should light.

K Set CAPACITANCE LOWER LIMIT switches 10 digits below proper value. Set CAPACITANCE and DISSIPATION/CONDUCTANCE UPPER LIMIT switches 10 digits above proper value. Set LIMIT RANGE switch one digit above proper range and initiate action of data source (on Type 1680-A, push START button); LOW C lamp should light.

If all checks passed, system is operating properly.

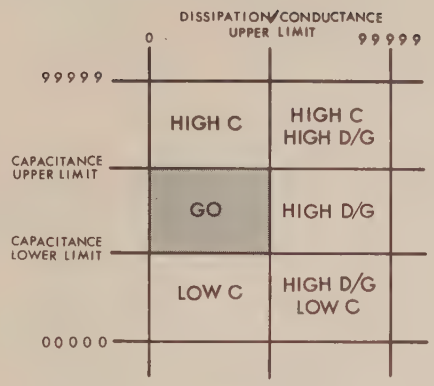
EXAMPLE



3.2 OPERATION

3.2.1 GENERAL

Principles. The Type 1781 Digital Limit Comparator is a digital calculator that automatically compares input measurement data with a set of limits and then provides an electrical and visual indication of the results of the comparison; GO if the input data is within the limits and NO GO if the input data exceeds the limits.



Three limits can be set, an upper and lower limit for capacitance and an upper limit for loss (dissipation factor or conductance). If the capacitance value is equal to or within the preset limits and if the loss is equal to or below the preset limit, the comparison result is in-tolerance and the GO lamp will light. If the capacitance value and/or the loss exceed the preset limits, the comparison result is out-of-tolerance and one of the NO GO lamps will light (LOW C or HIGH C and/or HIGH D/G).

If for some reason, a lower limit is not desired, set the lower-limit switches to 00000. And, similarly, if an upper limit is not desired, set the upper-limit switches to 99999.

DATA READY COMMAND CONTROL. This is a screwdriver-operated switch on the rear of the comparator that controls the output of the print command signal. The print command signal, PRT, initiates the operation of auxiliary equipment such as a printer, recorder, digital-to analog converter, another comparator, or other data processing devices, connected to the BCD DATA OUTPUT socket. The DATA READY COMMAND CONTROL has three positions:

1. PRINT ALL ---------- The external device is actuated after each comparison.
2. PRINT IN-TOLERANCE ONLY ---------- The external device is actuated only if the comparison resulted in a GO indication.
3. PRINT OUT-OF-TOLERANCE ONLY ---------- The external device is actuated only if the comparison resulted in a NO GO indication.

RANGE INFORMATION FOR TYPE 1680-A AUTOMATIC CAPACITANCE BRIDGE ASSEMBLY

RANGE	VOLTAGE	CAPACITANCE				LOSS			
	rms, across UNKNOWN	120 c/s MIN	120 c/s MAX	400 c/s, 1 kc/s MIN	400 c/s, 1 kc/s MAX	CONDUCTANCE MIN	CONDUCTANCE MAX	DISSIPATION FACTOR MIN	DISSIPATION FACTOR MAX
1	1 V			000.01 pF	150.00 pF	0000.1 n℧	1500.0 n℧	0.0000 D	1.5000 D
2	1 V			0150.0 pF	1500.0 pF	01.500 μ℧	15.000 μ℧	0.0000 D	1.5000 D
3	1 V			01.500 nF	15.000 nF	015.00 μ℧	150.00 μ℧	0.0000 D	1.5000 D
4	1 V	0000.1nF	1500.0nF	015.00 nF	150.00 nF	0150.0 μ℧	1500.0 μ℧	0.0000 D	1.5000 D
5	100 mV	01.500μF	15.000μF	0150.0 nF	1500.0 nF	01.500 m℧	15.000 m℧	0.0000 D	1.5000 D
6	10 mV	015.00μF	150.00μF	01.500 μF	15.000 μF	015.00 m℧	150.00 m℧	0.0000 D	1.5000 D
7	1 mV	0150.0μF	1500.0μF	015.00 μF	150.00 μF	0150.0 m℧	1500.0 m℧	0.0000 D	1.5000 D

3.2.2 MULTIPLE-GROUP SORTING (for equipment connections, see paragraph 2.9)

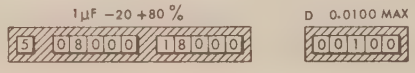
A single comparator can sort capacitors into six groups:

1. GO ---------- in-tolerance
2. LOW C ---------- capacitance below limit
3. HIGH C ---------- capacitance above limit
4. HIGH D/G ---------- loss above limit
5. LOW C and HIGH D/G ------ capacitance below limit and loss above limit
6. HIGH C and HIGH D/G ------ capacitance above limit and loss above limit

For example, an incoming lot of nominal 1-μF capacitors is to be checked for a tolerance of −20 +80% and a maximum D of 0.0100. Out-of-tolerance capacitors are to be rejected and returned to the manufacturer together with a record of their values.

If the data source is a Type 1680-A, set the LIMIT RANGE switch to 5 (from the table in paragraph 3.2.1).

Set the CAPACITANCE LOWER LIMIT switches to 1 μF - (0.2 x 1 μF) = 08000 and the CAPACITANCE UPPER LIMIT switches to 1 μF + (0.8 x 1 μF) = 18000.



Set the DISSIPATION/CONDUCTANCE UPPER LIMIT switches to 00100.

Since a record of out-of-tolerance values is necessary, a printer has been connected to the comparator and the DATA READY COMMAND CONTROL on the rear of the comparator is set to PRINT OUT-OF-TOLERANCE ONLY. If it was desired to send the manufacturer a record of all values for statistical analysis, but emphasize the out-of-tolerance values, the DATA READY COMMAND CONTROL could have been set to PRINT ALL and the RED/BLACK switch on the printer (if a Type 1137 Data Printer is used) could have been set to RED. In this way, all values would be printed; the in-tolerance values in black and the out-of-tolerance in red.

After all controls have been set, apply power to the system, perform the operational checks (if not yet performed, paragraph 3.1.2), and proceed with the measurements.

3.2.3 MULTIPLE-LIMIT SORTING (for equipment connections, see paragraph 2.9)

Several comparators can sort components into multiple-limit categories such as:

1. ±5%
2. ±10%
3. ±20%
4. reject

} or any other tolerances

For example, a production lot of nominal 100-pF capacitors is to be sorted into four categories; ±5%, ±10%, ±20%, and over 20%. Dissipation factor is unimportant.

Three comparators are required. Set the DATA READY COMMAND CONTROLS to PRINT OUT-OF-TOLERANCE ONLY (except for the last comparator on which it may be set to any position).

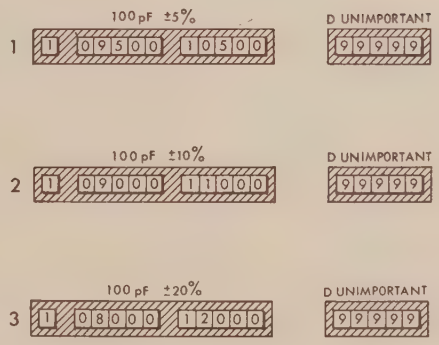
If the data source is a Type 1680-A, set the LIMIT RANGE switch to 1 (from the table in paragraph 3.2.1).

Since capacitors are not to be graded or rejected because of dissipation factor, set the DISSIPATION/CONDUCTANCE UPPER LIMIT switches to 99999.

On the first comparator, set the CAPACITANCE LOWER LIMIT switches to 100pF - (0.05 x 100pF) = 09500 and the CAPACITANCE UPPER LIMIT switches to 100pF + (0.05 x 100pF) = 10500.

On the second comparator, set the CAPACITANCE LOWER LIMIT switches to 100pF - (0.1 x 100pF) = 09000 and the CAPACITANCE UPPER LIMIT switches to 100pF + (0.1 x 100pF) = 11000.

On the third comparator, set the CAPACITANCE LOWER LIMIT switches to 100pF - (0.2 x 100pF) = 08000 and the CAPACITANCE UPPER LIMIT switches to 100pF + (0.2 x 100pF) = 12000.



After all controls have been set, apply power to the system, perform the operational checks (if not yet performed, paragraph 3.1.2), and proceed with the measurements.

Basic Principles

4.1 Basic Subtractor - - - - - - - - - - - - - 4-2
4.2 Block Description - - - - - - - - - - - - 4-4

Detailed Principles

4.3 Program Board - - - - - - - - - - - - - 4-6
4.4 Format Board ring-of-three - - - - - - - - 4-8
4.5 Ring-Of-Twelve Board - - - - - - - - - - 4-9
4.6 Parallel-Serial Boards - - - - - - - - - - 4-10
4.7 Format Board decimal-to-BCD converter - - - 4-12
4.8 Subtractor Board - - - - - - - - - - - - - 4-14
4.9 Relay and Relay Driver Boards - - - - - - - 4-17
4.10 Power Supply - - - - - - - - - - - - - - 4-18

4.1 BASIC SUBTRACTOR

The comparator uses a subtraction process to determine if an input is below, equal to, or above preset limits.

4.1.1 SIMPLE SUBTRACTION

Both decimal- and BCD-subtraction processes involve a borrow operation.

DECIMAL	BCD 8	4	2	1
	BORROW	BORROW		
12	1 0	1 0	1	1
- 7	- 0	1	0	1
5	0	1	1	0

For example, a decimal 3 is to be subtracted from a decimal 4.

4	0	1	0	0
- 3	- 0	0	1	1

The subtraction process starts with the least significant bit (1-bit). A borrow operation is performed first and then the actual subtraction.

			BORROW	
	0	1	0 - 1	1 0
	- 0	0	1	1
				1

The process is repeated for the next bit (2-bit).

		BORROW		
	0	1 - 1	1 0 - 1	1 0
	- 0	0	1	1
			0	1

A borrow operation is unnecessary for the third significant bit and only the subtraction process is carried out.

	0	1 - 1 - 0	1	1 0
	- 0	0	1	1
		0	0	1

A subtraction process is all that is necessary for the last bit after which the entire subtraction is complete.

	0	0	1	1 0
	- 0	0	1	1
1	0	0	0	1

4.1.2 BORROW SUBTRACTION

Borrow subtraction is the same as simple subtraction except the borrow terms are retained. For example, a decimal 3 is again to be subtracted from a decimal 4:

DECIMAL	BCD 8	4	2	1
4	0	1 (P = 1)	0 (P = 1)	0
- 3	- 0	0		
	0	0	0 (C = 1)	1 (C = 1)

C = current borrow. The 1-bit borrows from the 2-bit. This borrow is known as a current borrow, is retained in the answer, and is noted as C = 1.

P = previous borrow. The 2-bit was borrowed *from*. This borrow is known as a previous borrow and is noted as P = 1.

Since the 2-bit must also borrow, a current borrow is noted in the answer for its subtraction and a previous borrow is noted for the 4-bit. Since no borrows are necessary for the remainder of the subtraction process, no further borrow terms appear.

Rules. A set of rules for borrow subtraction can be formulated from the previous examples. Note that a 0 is used to denote the absence of a borrow and a 1 is used to denote its presence.

NO PREVIOUS BORROW				PREVIOUS BORROW			
0 (P = 0)	1 (P = 0)	0 (P = 0)	1 (P = 0)	0 (P = 1)	1 (P = 1)	0 (P = 1)	1 (P = 1)
- 0	0	1	1	0	0	1	1
0 (C = 0)	1 (C = 0)	[illegible]	0 (C = 0)	[illegible]	0 (C = 0)	[illegible]	[illegible]

Where the numbers subtracted from have no previous borrow, only one combination contains a current borrow in the answer; 0-1. But where the number subtracted from has been borrowed against (P = 1), only one combination is *without* a current borrow in the answer; 1 (P = 1) - 0.

4.1.3 COMPARISON

The comparator utilizes borrow subtraction to compare an input data signal to preset limits in order to determine if the input is smaller than, equal to, or larger than the limits.

	DECIMAL	BCD			
minuend	3	0	0	1	1
subtrachend	4	0	1	0	0
		1 (C = 1)	1 (C = 1)	1	1

For instance, in the previous example a smaller number was subtracted from a larger (4-3) and the answer contained no borrow term in the last column (8-bit). However, if a larger number is subtracted from a smaller (3-4), a borrow term is contained in the last column.

The two examples demonstrate three important facts:

1. **If no borrow term remains at the end of the subtraction, the minuend is equal to or larger than the subtrahend.**
2. **If a borrow term remains at the end of the subtraction, the minued is smaller than the subtrahend.**
3. **In order to determine if a borrow term remains or does not remain, it is necessary to carry the borrow terms from one column to the next; i.e., three pieces of information are necessary for the subtraction of each column, the two numbers and the previous borrow information.**

4.1.4 COMPARISON-LOGIC FORMULA

The borrow-subtraction rules can be expressed in a standard logic map as shown.

				①		②		③	④
PREVIOUS BORROW	P	0	0	0	0	1	1	1	1
FIRST NUMBER	Y	0	1	0	1	0	1	0	1
SECOND NUMBER	X	0	0	1	1	0	0	1	1
CURRENT BORROW	C	0	0	1	0	1	0	1	1
DIFFERENCE		0	1	1	0	1	0	0	1

The logic map can then be simplified to show only the conditions for C = 1 (current borrow present).

		P	Y	X
C = 1	1	0	0	1
	2	1	0	0
	3	1	0	1
	4	1	1	1

Since a 0 is the complement of a 1, the terms P = 0, Y = 0, and X = 0 can be written as $\overline{P}$, $\overline{Y}$, and $\overline{X}$. With this notation and the information from the map of C = 1, a complete logic equation for C can be written. Note that, in logic algebra, a multiplication indication such as XY actually means X and Y and that an addition indication such as X + Y actually means X or Y.

$$C = \overset{①}{\overline{P}}\overline{Y}X + \overset{②}{\overline{P}Y}\overline{X} + \overset{③}{P}\overline{Y}X + \overset{④}{PYX}$$

To simplify the logic equation, two terms are combined in such a manner as to result in a redundant expression. A redundant expression is one in which a variable appears with its complement; e.g., $X + \overline{X}$. Redundant expressions are absorbed and can be eliminated from the equation.

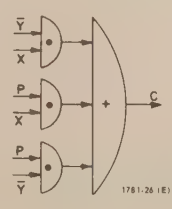
$$C = \overset{①}{\overline{P}}\overline{Y}X + \overset{③}{P}\overline{Y}X = \overline{Y}X(\overline{P} + P) = \overline{Y}X$$

$$C = \overset{③}{P}\overline{Y}X + \overset{④}{PYX} = PX(\overline{Y} + Y) = PX$$

$$C = \overset{②}{P}\overline{Y}\overline{X} + \overset{③}{P}\overline{Y}X = P\overline{Y}(\overline{X} + X) = P\overline{Y}$$

The simplified expression is then used as the basis for the electronic circuitry that must perform the subtraction. Note that if any two of the three different inputs ($\overline{Y}$, X, and P) are true, C is true.

$C = \overline{Y}X + PX + P\overline{Y}$



Simplified logic representation.

① MAJORITY AND-GATE: ONLY TWO INPUTS NEED BE TRUE FOR A TRUE OUTPUT.

4.2 BLOCK DESCRIPTION

Diagram AQ.

4.2.1 GENERAL

The instrument uses a subtraction process to determine if the input data is below, equal to, or above preset limits. Two subtractors are used, one for the upper limits of loss and capacitance and one for the lower limit of capacitance. Each subtractor performs the subtraction serially; i.e., one digit (4-bits) at a time.

Since the input data source and the preset limits in the instrument present their information in parallel (all digits simultaneously), a parallel-to-serial converter is used to convert the information to serial form for use by the subtractors. And since one of the subtractors processes both loss and capacitance, additional circuitry is used to store the result of one complete subtraction before proceeding to the next.

At the end of the subtraction, the results are displayed visually by means of front-panel lamps which indicate GO or NO GO and the reason for NO GO (LOW C, HIGH C, or HIGH D).

In order to start the comparison process when the input data source is ready, the comparison is initiated by the data source. And in order to synchronize the various operations, all circuits in the comparator are synchronized by a clock generator that provides clock pulses at a 20-Hz rate.

4.2.2 PRESET

Initiate. The 1-0 transition of the **STA** compare initiate signal from the input data source (PRT′ from the Type 1680) initiates the action of the circuits on the program board.

Preset. Before the start of the comparison, **RE1** is 0 which disables the **ARC3** clock pulses and prevents the comparator from operating. The STA compare initiate signal sets **R3** to 1 and R3 sets the ring-of-three circuit to its third position, **RE2**, which sets the memory flip-flops on the parallel-serial board to 0. The STA signal also sets **R12** to 1 which sets the ring-of-twelve board to its twelve position, **L**. STA also sets **LPGP** to 1 which enables the relay drivers so that the appropriate relay and lamp (GO, LOW C, HIGH C, or HIGH D) can be energized at the end of the comparison.

4.2.3 ADVANCE AND TRANSFER (parallel-to-serial conversion)

Advance. After 800μs, **RE1** changes to 1 and allows the clock generator to operate. The first **ARC3** clock pulse advances the ring-of-three to its next position, **ARC12**, and the ARC12 signal advances the ring-of-twelve to its first position, **A**.

Transfer. The **A** signal enables the 4-bit BCD information from the least significant loss digits (decade D4 on the B side of the Type 1680) to be transfered into the memory flip-flops on the parallel-serial board and then on to the upper subtractor.

The A signal also enables the decimal information from the least significant digit of the preset upper loss limit to be transfered to the decimal-to-BCD convertor on the format board and then on to the upper subtractor.

4.2.4 SUBTRACT AND STORE BORROW

Subtract. The upper subtractor subtracts the least-significant digit of the loss input data from the least-significant digit of the upper limit.

Store borrow. The next **ARC3** clock pulse advances the ring-of-three to its next position, **STB**. STB causes the upper subtractor to store any borrow term that may have resulted from the first-digit subtraction and hold it as the previous borrow for the next-digit subtraction.

4.2.5 REPEAT

The next **ARC3** clock pulse advances the ring-of-three to its third position, **RE2**. RE2 resets the memory flip-flops to 0 to prepare for the subtraction of the next figure. The next ARC3 clock pulse advances the ring-of-three to **ARC12** which advances the ring-of-twelve to its second position, **B**.

The B signal transfers the second significant figure of the input data and limit setting to the subtractor, the next ARC3 clock pulse causes the store-borrow operation, and so on until the ring-of-twelve reaches its sixth position, **F**.

4.2.6 SHIFT AND CONTINUE

The **F** signal enables two 2-input and-gates.

Store loss. In the first gate, the second input is the **STB** signal and the output, **STBD**, causes the upper subtractor to shift any borrow term that may have resulted from the subtraction, out of the subtractor itself and into a memory circuit. This allows the subtractor to proceed from the completed loss subtraction to the capacitance subtraction. The borrow term, **(BOS)** if present, is then still available to drive the appropriate lamp (**HIGH D** in this case).

Clear subtractor. In the second gate, the second input is the **RE2** signal and the output causes the upper subtractor to erase any borrow term after it has shifted it to the memory.

Continue. The advance-and-transfer and subtract-and-store-borrow operations continue until the subtractions of the entire five-digit capacitance signals and single-digit range signal are complete. Any borrow terms that may have resulted (**B0** or **ZB0**) are sent to the relay drivers which energize the appropriate lamp (**HIGH C** or **LOW C**). If no borrow terms are present, the GO lamp is energized.

4.2.7 STOP

Stop. The last position of the ring-of-twelve, **L**, enables a 2-input and-gate. The second input is **RE2** and the output, **RE1**, disables the clock generator and stops the **ARC3** clock pulse which stops the comparator operation.

Print command. **RE1** also causes a 1-0 transition of the **PRT** print command signal which is applied to the DATA OUTPUT socket, SO32 on the rear of the comparator, and initiates the operation of a printer, digital-to-analog converter, or other piece of data processing equipment that may be connected to the socket.

4.3 PROGRAM BOARD

Diagram G. The program board provides the signals to preset the circuits before each comparison and provides the signals to start each comparison.

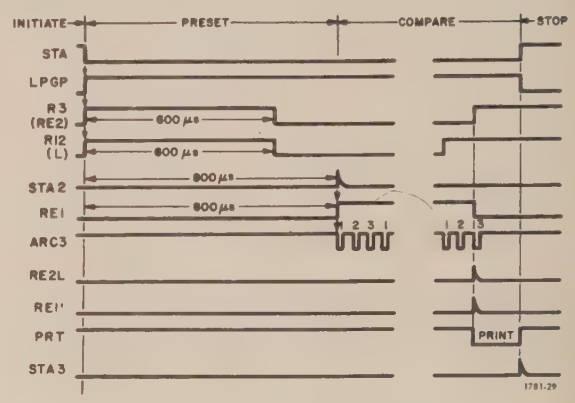
4.3.1 PRESET

STA. A compare initiate signal from the input data source (PRT′ from the Type 1680) is applied to the STA input of the comparator. The STA signal connects to the base of Q401, the input emitter follower, which drives the start Schmitt.

LPGP. One output of the start Schmitt is the LPGP signal which connects to the driver enable amplifier on the relay driver board and provides the relay and lamp drivers with a negative return.

R3. The 0-1 LPGP transition passes through C407 and CR404 to the base of Q405 in the 800-μs delay circuit. Q405 turns off which turns on Q404 and Q414. The 1-level Q414 emitter signal passes through C413 to the base of Q415 which turns off and remains off for the duration of the RC time of C413 and R446 (about 600μs).

When Q415 turns off, it back-biases CR408. Q416 base potential is then determined by the divider action of R448, CR409, and R449 which places Q416 base sufficiently negative to turn on Q416 and set R3 to 1. The 1-level R3 signal sets the ring-of-three circuit on the format board to its last position RE2, which presets the memory flip-flops on the parallel-serial boards to 0.



R12. The R12 signal is derived in the same manner as the R3 signal except the output transistor is Q417 and the signal sets the ring-of-twelve board to its last position.

4.3.2 START

STA2. After 800μs, the 800-μs delay circuit returns to its stable state, Q405 again conducts, and its collector goes to the 1-level. The 0-1 transition at Q405 collector (STA2 signal) passes through C408 and CR403 to the base of Q409 in the reset flip-flop.

RE1. Before the start of a comparison, Q409 is on which places RE1 at a 0-level. 800μs after the compare initiate signal, STA2 turns off Q409 which turns on Q408 and sets RE1 to 1.

ARC3. When RE1 is 1, it allows the clock generator, a freerunning multi, to oscillate and produce 20-kHz clock pulses (ARC3 signal) which drive the ring-of-three circuit of the format board and start the actual comparison operation.

4.3.3 STOP

RE2L. When the ring-of-twelve board reaches its last position, it causes a 1-level **R12** signal which passes through R437 in the R12 amplifier and zero-biases CR407. When the ring-of-three circuit on the format board reaches its last position, it causes a 1-level **RE2** signal, the 0-1 transition of which (**RE2L** signal) passes through CR407 to the base of Q408 in the reset flip-flop and turns off Q408. When Q408 turns off it sets **RE1** to 0 which disables the clock generator, stops the **ARC3** clock pulses, and thus stops the comparison operation.

RE1′. When Q408 turns off, Q409 turns on and the 0-1 transition (RE1′ signal) passes through C404 and CR402 to the base of Q407 in the print-command flip-flop.

PRT. The **RE1′** signal turns off Q407 and sets PRT to 0. Thus, a new print command is generated approximately 2.5 ms (the duration of the comparison) after the old (STA) was received. It is used to initiate a printer, another comparator, digital-to-analog converter, or other piece of data processing equipment after the comparison has been made.

DATA READY COMMAND CONTROL. The occurance of a **PRT** signal is controlled by the DATA READY COMMAND CONTROL, S903 on the rear of the instrument. If this switch is set to PRINT ALL, CR402 anode is returned to ground which zero-biases CR402 and allows **RE1'** signals to set PRT to 0 after each comparison.

But if S903 is set to PRINT IN-TOLERANCE ONLY, CR402 is zero-biased only if the **CK** signal from the relay driver board is at a 1-level which only occurs if the comparison resulted in a GO (in-tolerance) measurement. Simiarily, if S903 is set to PRINT OUT-OF-TOLERANCE ONLY, a **CKK** signal is required to zero-bias CR402 and a CKK signal occurs only if the comparison resulted in a NO GO (out-of-tolerance) measurement.

STA3. When the **STA** compare initiate signal returns to the 1-level, the 0-1 transition (STA3 signal) passes through CR402 and CR401 to the base of Q401 in the print command flip-flop and turns off Q406. When Q406 turns off, Q407 turns on and sets **PRT** to 1.

4.3.4 COMPARE BUTTON

STAB. The COMPARE button, S904 on the front panel, is used to initiate comparisons without creating PRT print commands. The button works in conjunction with the **STA** compare initiate input which must be 0 (indicating the input data source is ready) before any comparisons are initiated.

Before the COMPARE button is pushed, Q412 and Q413 are off. When the button is pushed, STAB is connected to ground which turns on Q412 and, by means of the regenerative connection to Q413 base, turns on Q413. When Q413 turns on, its collector goes to the 1-level and the 0-1 transition performs the same action as did the 0-1 transition of the LPGP signal; i.e., initiates the 800-μs and 600-μs delay circuits which, in turn, preset the comparator and then start the comparison operation.

After the COMPARE button is released, C411 retains the 1-level charge on Q412 base for the duration of the time constant of C11, R441, and R443 (about 30ms). Thus, the potential at Q413 collector is a positive pulse that is unaffected by any contact bounce of S904.

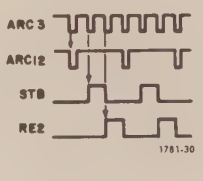
4.3.5 UNWANTED PRINT COMMAND

STA1. When the 800-μs delay is initiated, Q404 turns on and its collector goes from 0 to 1. This 0-1 transition (STA1 signal) passes through C409 and CR406 to the base of Q408 in the reset flip-flop. Ordinarily, before a comparison is made, Q408 is off. However, when the comparator is first turned on, Q408 may be on in which case the STA1 signal is used to turn it off so that a proper comparison operation can be carried out.

But if Q408 is turned off by **STA1**, Q409 would go from 0 to 1 and the 0-1 transition (RE1' signal) would be applied to CR402 before the start of a comparison rather than after it. Since it is also possible that CR402 is zero-biased by a **CK** or **CKK** signal which has not yet assumed the correct level (because no comparison has been completed), the STA1 signal may pass through CR402 and set **PRT** to 0.

Thus, the first comparison made after the instrument is turned on may result in a print command regardless of the setting of the DATA READY COMMAND CONTROL. The comparison result is accurate however, as is the print-out, and the anomaly can occur only on the first comparison after power has been applied. There is no deviation from normal operation on subsequent comparisons and no deviations at all if the DATA READY COMMAND CONTROL is set to PRINT ALL.

Diagram H. Format board also described in paragraph 4.7. The ring-of-three circuit on the format board sequences the various operations involved in the comparison process:



ARC12. The first position is ARC12 which advances the ring-of-twelve board and thus transfers the input-data and preset-limit figures, one digit at a time, into the subtractors.

STB. The second position is STB which stores the borrow information, if any, from each subtraction.

RE2. The third position is RE2 which clears the memory flip-flops on the parallel-serial board and thus prepares them for the subtraction of the next digit.

4.4.1 QUIESCENT

The **ARC3** signal is normally at the 1-level which allows Q101, the advance amplifier, to conduct and provide a negative return for each of the three flip-flops in the ring-of-three circuit, Q102 and Q103, Q104 and Q105, and Q108 and Q109. Only one flip-flop at a time is energized, however, and for the moment assume it is the first or ARC12 flip-flop, Q102 and Q103.

4.4.2 ADVANCE

When a negative **ARC3** signal arrives, Q101 turns off which deprives Q102 of its negative return and it also turns off. When Q102 turns off, its collector goes to the 1-level which turns off Q103. The resultant 1-0 transition at Q103 collector passes through C101 to the base of Q104 in the next flip-flop.

By this time, the ARC3 pulse has decayed and Q101 is again allowed to conduct and provide a negative return for the flip-flops. Thus, when Q104 receives the 1-0 at its base, it turns on and its collector goes to the 1-level which also turns on Q105. Since no other flip-flop received a trigger, the second flip-flop is the only one to be energized.

The next ARC3 pulse turns off Q104 and Q105 and turns on Q108 and Q109 which sets RE2 to 1. The next ARC3 pulse deenergizes RE2 and energizes ARC12 and so on until the ARC3 clock pulses are disabled.

4.5 RING-OF-TWELVE BOARD

Diagram I. The ring-of-twelve board provides the signals necessary to convert the parallel information from the input data source and from the limit switches to serial information for use by the subtractors. Each position of the ring-of-twelve provides at least three outputs: one for the parallel-serial boards to convert the input data to serial information, one to the lower-limit switches to convert the lower limits to serial information, and one to the upper-limit switches to convert the upper limits to serial information.

4.5.1 OPERATION

The operation of the ring-of-twelve is identical to the operation of the ring-of-three circuit on the format board (paragraph 4.4) except the advance amplifier is driven by the **ARC12** signal from the ring-of-three.

Diagram J. The parallel-serial boards convert the parallel BCD information from the data input source to serial information for use by the subtractors. Two boards are used, one for the 1- and 2-bits and one for the 4- and 2′- (or 8) bits; both boards are identical.

4.6.1 START

A1 through A4, B1 through B4. After the input data source completes a measurement, it presents its data to the BCD DATA INPUT socket, SO32 on the rear of the comparator. Although the source can present up to eleven digits, only two are shown (A and B which, from the Type 1680, are the first two loss digits). In the figure, A is a decimal 3 (binary 1100) and B is a decimal 6 (binary 0110).

ARC3. When the input data source is ready, it issues a compare initiate signal (STA) and 800μs later ARC3 clock pulses from the program board (paragraph 4.3) initiate the comparison operation.

ARC12. The ARC3 clock pulses drive the ring-of-three circuit on the format board (paragraph 4.4). The first position of the ring-of-three is ARC12.

4.6.2 ADVANCE AND TRANSFER (parallel-to-serial conversion)

AA. The first ARC12 pulse sets the ring-of-twelve board (paragraph 4.5) to its first position, AA.

The signals from the input data source and the ring-of-twelve are applied to 2-input and-gates on the parallel-serial boards. The A inputs from the input data source arrive first. If an A input is 1, it zero-biases the associated diode so that when the AA signal from the ring-of-twelve arrives, the 0-1 transition passes through the capacitor and diode to the memory flip-flop and sets the flip-flop to 1.

X1. The A input is a decimal 3 (binary 1100), therefore the first bit, A1, is 1 and zero-biases CR702 on the rear parallel-serial board. When the AA signal arrives, the 0-1 transition passes through C702 and CR702 to the base of Q702 in the memory flip-flop. Q704 turns off and Q703 turns on which sets X1 to 1.

ZX2. The second bit, A2, is also 1 and zero-biases CR701. When AA arrives, the 0-1 transition turns off Q702 which turns on Q701 and sets ZX2 to 1.

X4. The third bit, A3, is 0 and does not zero-bias CR702 on the front parallel-serial board. The 0-1 transition of the AA signal, therefore, cannot pass through CR702 and the output of the memory flip-flop, X4, remains 0.

ZX8. The fourth bit, A4, is also 0 so that ZX8 also remains 0.

The signal from the ring-of-twelve board thus transfers all four bits of the first digit from the input data source to the memory flip-flops.

4.6.3 SUBTRACT AND STORE BORROW

The outputs from the memory flip-flops are applied to the subtractor board which performs the actual comparison (subtraction).

STB. The second position of the ring-of-three, STB, is also applied to the subtractors (paragraph 4.8.2) and is used to store any borrow term that may have resulted from the subtraction.

RE2. The 0-1 transition of the third position of the ring-of-three, RE2, clears the memory flip-flops (sets their outputs to 0) in preparation for the transfer of the next digit.

4.6.4 REPEAT

After its third position, the ring-of-three returns to its first position and produces another ARC12 pulse which advances the ring-of-twelve to its next position, BB.

The BB signal transfers all four bits of the second figure from the input data source to the memory flip-flops in the same manner as before. The borrow term, if any, is stored by the STB signal after which the RE2 signal clears the memory flip-flops in preparation for the next transfer, CC.

Summary. The figures from the input data source are presented to the subtractors, one digit at a time, by the parallel-serial boards (parallel-to-serial conversion). Each complete transfer requires three positions of the ring-of-three circuit which is stepped at a rate of approximately once each 50μs, therefore approximately 150μs are required to complete the subtraction of one digit. Since there are twelve positions, about 1.7 ms are required to complete the subtraction of all digits plus the 800-μs preset delay which amounts to a total comparison time of 2.5 ms.

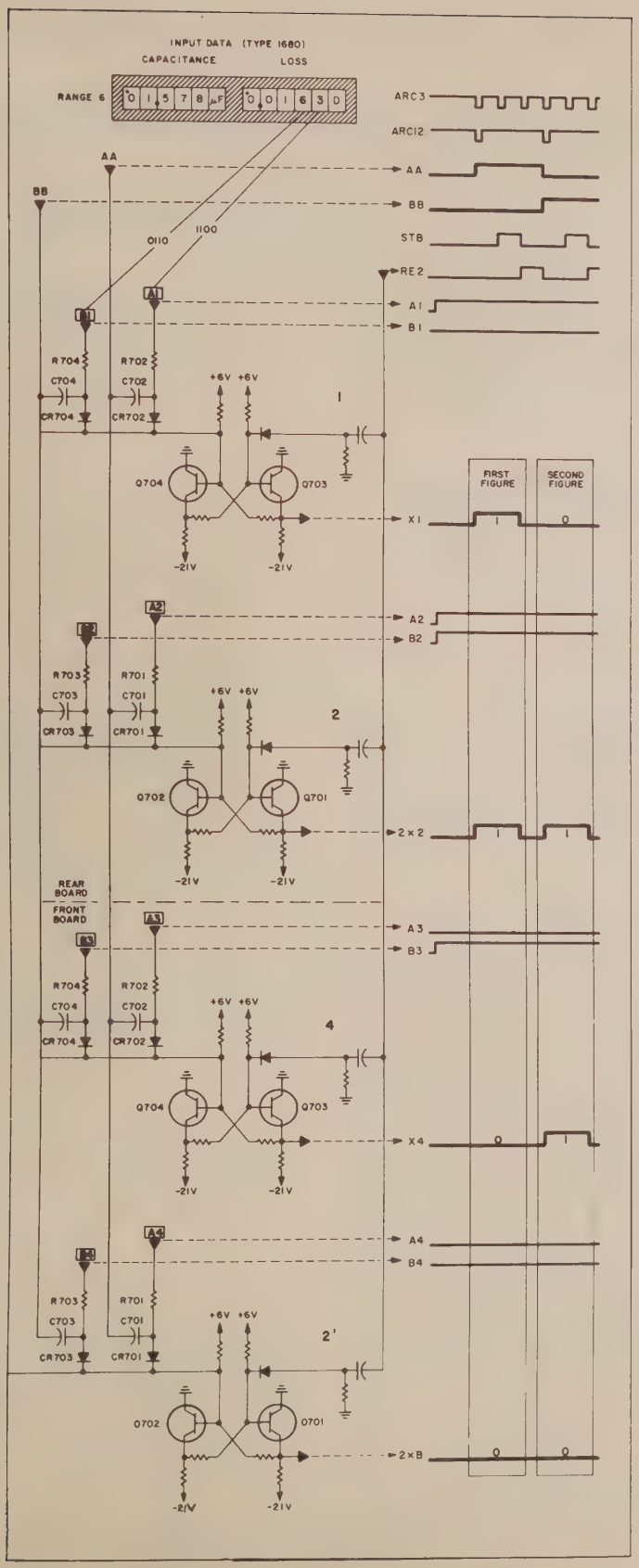

INPUT DATA (TYPE 1680)
CAPACITANCE
LOSS
RANGE 6
0 1 5 7 8 μF
0 0 1 6 3 0
ARC3
ARCI2
AA
BB
0110
1100
ST8
RE2
A1
B1
R704
R702
C704
C702
CR704
CR702
+6V
1
Q704
Q703
-21V
FIRST FIGURE
SECOND FIGURE
X1
A2
B2
R703
R701
C703
C701
CR703
CR701
2
Q702
Q701
2 x 2
REAR BOARD
FRONT BOARD
A3
B3
4
X4
A4
B4
2'
2xB

Diagram H. Format board also described in paragraph 4.4. In addition to the ring-of-three circuit (paragraph 4.4), the format board also contains decimal-to-BCD converters for the limit information. These converters accept the parallel decimal information from the LIMIT switches, S901 and S902 on the front panel, and convert it to serial BCD for use by the subtractors.

4.7.1 BCD CHANGE

In order to electrically perform the logic equation for comparison ($C = \overline{Y}X + PX + P\overline{Y}$, paragraph 4.1.4) and for electrical convenience in the subtractor, the limit information to the subtractor must be changed from the normal 1-2-4-2′ BCD to $\overline{1}$-2-$\overline{4}$-2′ BCD; i.e., the odd bits are complemented.

DECIMAL	NORMAL				ODD-BIT COMPLEMENTED			
	1	*2*	*4*	*2*	*1*	*2*	*4*	*2′*
0	0	0	0	0	1	0	1	0
1	1	0	0	0	0	0	1	0
2	0	1	0	0	1	1	1	0
3	1	1	0	0	0	1	1	0
4	0	0	1	0	1	0	0	0
5	1	0	1	0	0	0	0	0
6	0	1	1	0	1	1	0	0
7	1	1	1	0	0	1	0	0
8	0	1	1	1	1	1	0	1
9	1	1	1	1	0	1	0	1

4.7.2 START

AA1 and BB1. Before the comparison is made, the LIMIT switches are set for the desired limits. Although there are eleven switches, only two are shown (AA and BB which are the first two limit switches for loss). In the figure, the AA1 wiper has been set to a decimal 4 (odd-bit-complemented binary 1000) and the BB1 wiper has been set to a decimal 5 (odd-bit-complemented binary 0000).

AC3. When the input data source is ready, it issues a compare initiate signal (STA) and 800μs later ARC3 clock pulses from the program board (paragraph 4.3) initiate the comparison operation.

ARC12. The ARC3 clock pulses drive the ring-of-three circuit on the format board (paragraph 4.4). The first position of the ring-of-three is ARC12.

4.7.3 ADVANCE AND TRANSFER (parallel-to-serial conversion)

AA1. The first ARC12 pulse sets the ring-of-twelve board (paragraph 4.5) to its first position, AA1.

The output from the first position of the ring-of-twelve board is applied to the wiper of the first switch for the loss figures where it passes through diodes to the appropriate BCD line or lines.

U1C. The 1-level AA1 input is connected to the decimal-4 position of the LIMIT switch where it passes through CR105 and sets the U1C line (complemented 1-bit) to 1.

U2, U4C, U8. The decimal-4 position of the LIMIT switch contains no diodes to the other BCD lines, therefore these lines (2-bit, complemented 4-bit, and 2′-bit) remain 0.

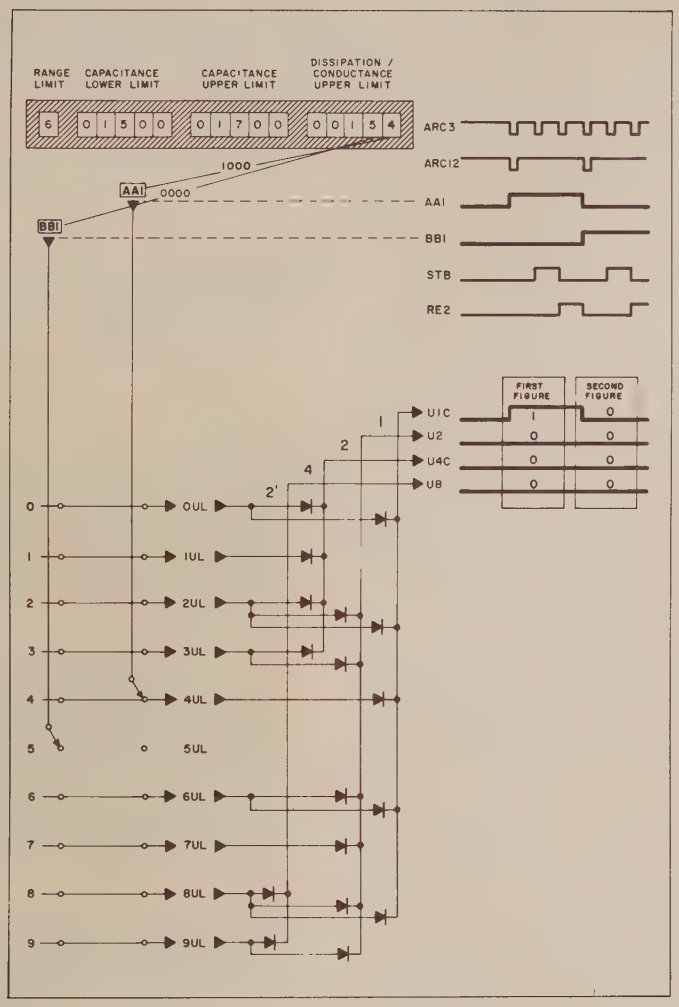
The signal from the ring-of-twelve thus converts the decimal figure from the LIMIT switch to a BCD figure and transfers it from the LIMIT switch to the four BCD lines.

4.7.4 SUBTRACT AND STORE BORROW

The BCD lines are connected to the subtractor board which performs the actual comparison (subtraction).

STB. The second position of the ring-of-three, STB, is also applied to the subtractors (paragraph 4.8.2) and is used to store any borrow term that may have resulted from the subtraction.

RE2. The third position of the ring-of-three, RE2, clears the memory flip-flops on the parallel-serial boards (paragraph 4.6.3) in preparation for the transfer of the next figure from the input data source.



4.7.5 REPEAT

After its third position, the ring-of-three returns to its first position and produces another ARC12 pulse which advances the ring-of-twelve to its next position, BB1.

The BB1 signal converts and transfers the second digit of the loss limit in the same manner as before. The borrow term, if any, is stored by the STB signal after which the RE2 signal clears the memory flip-flops on the parallel-serial boards in preparation for the next transfer, CC1.

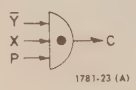
Summary. The decimal figures from the LIMIT switches are converted, one digit at a time, by the decimal-to-BCD converters on the format board. The conversion time is the same as the comparison time (2.5 ms) as noted at the end of paragraph 4.6.4.

4.8 SUBTRACTOR BOARD

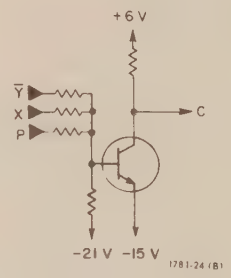
Diagram K. There are two subtractor circuits on the subtractor board, an upper and a lower; both are identical. The upper subtractor first subtracts the loss figures of the input data from the loss figures of the upper-limit switches. Then as the ring-of-twelve advances, it subtracts the capacitance figures of the input data from the capacitance figures of the upper-limit switches. The lower subtractor subtracts the capacitance figures of the lower-limit switches from the capacitance figures of the input data.

4.8.1 BASIC SUBTRACTOR

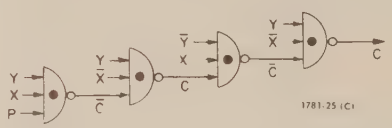
Majority and-gate. In paragraph 4.1.4 it was learned that the basic unit in the subtractor circuit is the 3-input majority and-gate; if any two of the inputs are true (1), the output is true (1).



Majority nand gate. In practice, this gate is not an and-gate, it is a nand-gate; i.e., because of the transistor output, the output signal is inverted (complemented) with respect to the input so that if any two inputs are true (1), the output is not true (0).



4-bit subtractor. Each gate performs a subtraction on one bit of the BCD input, therefore four cascaded gates are required to perform a complete subtraction on the 4-bit inputs. Since the output of each gate is inverted, every other gate must operate with the complement of the signals applied to the first gate; $\overline{Y}$ is complemented to Y, X to $\overline{X}$, and P (previous borrow) to $\overline{C}$ (current borrow).



Y odd-bit complemented. In paragraph 4.7.1 it was noted that the limit data presented to the upper subtractor is not a normal BCD code but is changed so that the first and third (odd) bits were complemented. This is done for two reasons: first because the logic expression uses the $\overline{Y}$ function and, second, because the subtractor uses nand gates so that the inputs to every other gate must be complemented. The net result is that the odd bits of the Y information to the subtractors are complemented.

DECIMAL	NORMAL BCD	Y ODD-BIT COMPLEMENTED	X EVEN-BIT COMPLEMENTED
0	0 0 0 0	1 0 1 0	0 1 0 1
1	1 0 0 0	0 0 1 0	1 1 0 1
2	0 1 0 0	1 1 1 0	0 0 0 1
3	1 1 0 0	0 1 1 0	1 0 0 1
4	0 0 1 0	1 0 0 0	0 1 1 1
5	1 0 1 0	0 0 0 0	1 1 1 1
6	0 1 1 0	1 1 0 0	0 0 1 1
7	1 1 1 0	0 1 0 0	1 0 1 1
8	0 1 1 1	1 1 0 1	0 0 1 0
9	1 1 1 1	0 1 0 1	1 0 1 0

X even-bit complemented. The input data presented to the upper subtractor are also changed because of the nand gates. This time the even bits are complemented and the complementing takes place in the memory flip-flops on the parallel-serial boards. The output to the upper subtractor is taken from the odd transistor for the (X1 and X4) and from the even transistors for the second and fourth bits (even bits, X2C and X8C) which are complemented.

Complemented inputs. The Y input to the subtractors is always odd-bit complemented and the X input is always even-bit complemented. Since the upper subtractor subtracts the input data from the limit, the limit is Y and is odd-bit complemented and the input data is X and is even-bit complemented. And since the lower subtractor subtracts the limit from the input data (just the reverse of the upper subtractor), the input data is Y and is odd-bit complemented and the limit is X and is even-bit complemented.

INPUT	BCD COMPLEMENTED	SUBTRACTOR UPPER	SUBTRACTOR LOWER
Y minuend	ODD-BIT	LIMIT	INPUT
− X subtrahend	EVEN-BIT	INPUT	LIMIT

4.8.2 SUBTRACTION EXAMPLE Upper subtractor (Upper limit – input data)

Start. 800μs after the STA compare initiate signal is applied, **RE1** from the program board goes to the 1-level. The 0-1 transition of RE1 passes through C202 to the base of Q202 in the high C borrow-memory which turns off Q202 and sets **BO** to 0. Thus, the borrow input to the first gate is 0.

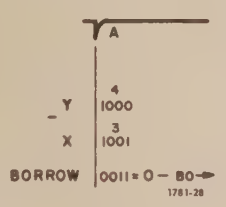
The 0-1 transition of **RE1** also passes through C203 to the base of Q203 in the high D memory and sets **BOS** to 0.

The 1-level of **RE1** allows the clock generator on the program board to produce **ARC3** clock pulses. The first ARC3 clock pulse sets the ring-of-three circuit on the format board to its first position, **ARC12.**

Advance and transfer. The first **ARC12** pulse sets the ring-of-twelve board to its first position, **A.** The A outputs (**AA1** and **AA**) from the ring-of-twelve transfer the first digit of loss (dissipation factor or conductance) from the LIMIT switch and the data input to the majority gates in the upper subtractor.

Subtract and store borrow. In the example, the first digit of the loss upper limit is a decimal 4 which is presented to the subtractor as the odd-bit-complemented **Y** input. And the first digit of the loss input data is a decimal 3 which is presented to the subtractor as the even-bit complemented **X** input. The borrow input, **P**, is BO which has been set to 0 by the RE1 signal.

Since the majority of inputs to the first gate are 1 (the only 0 is the borrow), the output is 0 which is presented to the next gate as the borrow input (current borrow, C). The majority of inputs to the second gate are 0 so the output is 1 which is presented to the next gate and so on until the last gate produces an output which, in this example, is 0.



The 0-level output of the last gate (Q208 collector) zero-biases CR211 in the base of Q202 in the high C borrow memory. The next position of the ring-of-three is **STB.** With CR211 zero-biased, the 0-1 transition of the STB signal passes through CR211 and C205 to the base of Q202 which turns off Q202 and sets **BO** (previous borrow, P) to 0.

The third position of the ring-of-three, **RE2,** clears the memory flip-flops on the parallel-serial boards in preparation for the subtraction of the next digit.

Repeat. After its third position, the ring-of-three returns to its first position and produces another ARC12 pulse which advances the ring-of-twelve to its next position, B.

The B outputs transfer the second digit of the loss upper limit and the loss data input to the subtractors where they are subtracted as before and where the borrow is stored as before. This process continues through position E of the ring-of-twelve which completes the subtraction of the loss figure.

In this example, a borrow term was left at the output of the last gate after the complete subtraction of the loss figure which means the input data exceeded the limit. The 1-level output of the last gate (Q208 collector) zero-biases CR209 in the base of Q205 in the high C borrow memory. The next position of the ring-of-three is STB. With CR209 zero-biased, the 0-1 transition of the STB signal passes through C206 and CR209 to the base of Q205 which turns off Q205, turns on Q202, and sets BO to 1.

Shift and continue. The ring-of-twelve advances to its **F** position. The F signals are not applied to the format board and no input data is applied to the F positions on the parallel-serial boards, hence the F position transfers no digits to the subtractor.

Instead, an F signal (**FF3**) is applied to CR103 in the base of Q112 of the borrow-transfer flip-flop on the format board and zero-biases CR103. When the ring-of-three advances to **STB**, the 0-1 STB transition passes through C106 and CR103 to the base of Q112 which turns off Q112 and sets **STBD** to 0. After 25 μs, the RC time constant of R122 and C107 returns Q112 to conduction and sets STBD back to 1.

The 1-level BO signal zero-biases CR210 in the base of Q204 of the high D borrow memory so that the 0-1 **STBD** transition passes through C204 and CR210 which turns off Q204, turns on Q203 and sets **BOS** to 1. The BOS signal drives the high D driver on the relay driver board which energizes the HIGH D lamp on the front panel.

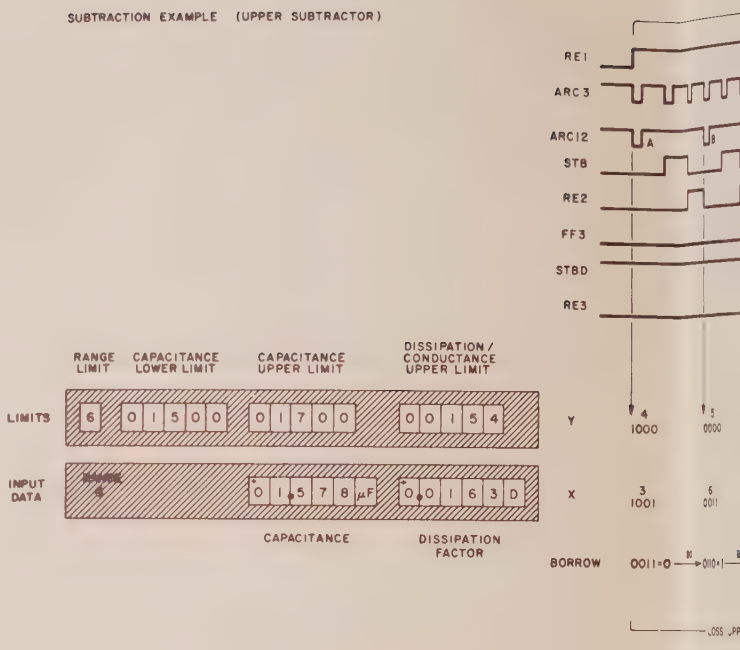
FF3 also zero-biases CR202 in the base of Q202 of the high C borrow memory. When the ring-of-three advances to **RE2**, the 0-1 RE2 transition passes through C201 and CR202 to the base of Q202 which turns off Q202 and sets **BO** to 0.

Thus, the FF3 signal shifts the result of the first complete subtraction to the High D borrow memory and clears the high C borrow memory in preparation for the next complete subtraction.

The next positions of the ring-of-twelve (**G** through **L**) transfer the upper limit digits and input data digits of capacitance, including range, to the upper subtractor where the subtraction operations are performed in the same manner as with the loss figures. Positions G through L also transfer the lower limit digits and input data digits to the lower subtractor where the same subtraction operations are performed except the limit and input data inputs are reversed, Y is the input data and X is the limit so that the limit is subtracted from the input data.

Stop. The **L** position of the ring-of-twelve also provides a signal, **R12**, which zero-biases CR407 in the base of Q408 of the reset flip-flop on the program board. When the ring-of-three advances to **RE2**, the 0-1 RE2 transition passes through C410 and CR407 to the base of Q408 which turns off Q408 and sets **RE1** to 0. A 0-level RE1 signal disables the clock generator which stops the **ARC3** clock pulses and stops the comparison operation.

Any borrows which resulted from the subtractions are left in the borrow memories to drive the relay drivers; i.e., if **BO, BOS,** or **ZBO** are 1, indicating an out-of-tolerance measurement, they energize their respective driver which, in turn, energize the appropriate front-panel NO GO lamp.



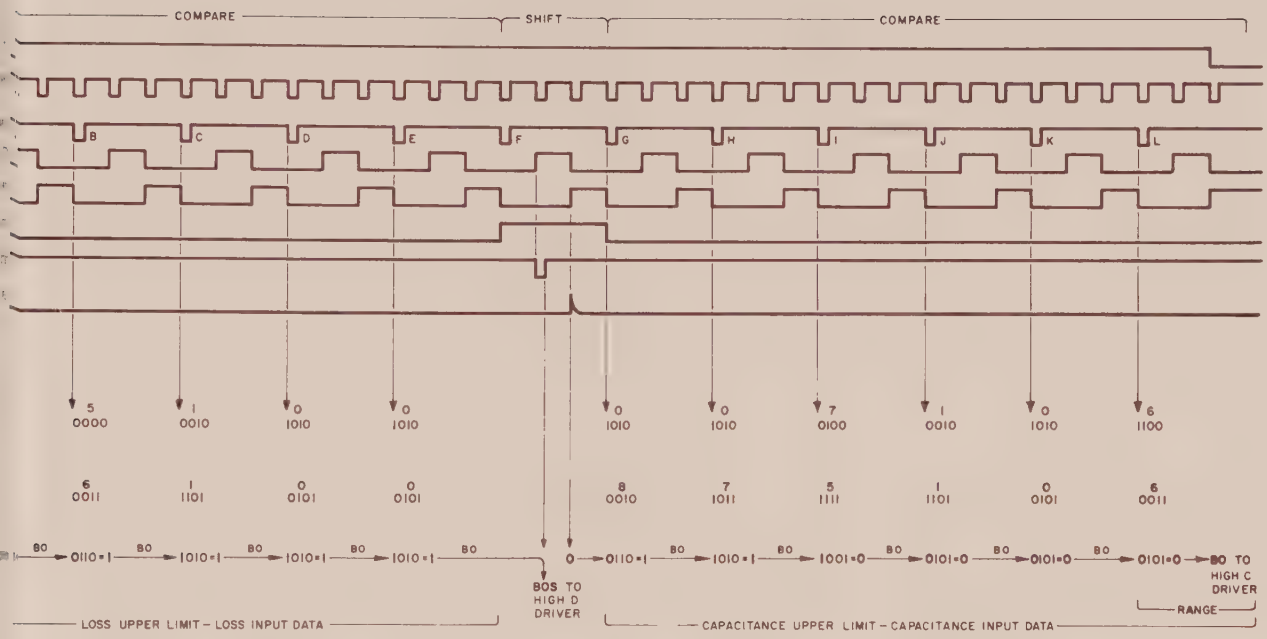

COMPARE
SHIFT
COMPARE
B
C
D
E
F
G
H
I
J
K
L
5 0000
1 0010
0 1010
0 1010
0 1010
0 1010
7 0100
1 0010
0 1010
6 1100
6 0011
1 1101
0 0101
0 0101
8 0010
7 1011
5 1111
1 1101
0 0101
6 0011
BO
0110-1
1010-1
1010-1
1010-1
0
0110-1
1010-1
1001-0
0101-0
0101-0
0101-0
BO TO HIGH C DRIVER
BOS TO HIGH D DRIVER
RANGE
LOSS UPPER LIMIT – LOSS INPUT DATA
CAPACITANCE UPPER LIMIT – CAPACITANCE INPUT DATA

Diagram L. The relay driver board uses the borrow information from the subtractor board to energize the front-panel lamps which provide a visual indication of the result of the comparison. The relay drivers also energize relays on the relay board which provide contact closures to drive external sorting equipment.

4.9.1 NO GO, OUT-OF-TOLERANCE

A 1-level borrow signal (**ZBO, BO,** or **BOS**) from the subtractor board turns on the appropriate driver transistor (Q308, Q305, or Q309) on the relay driver board which energizes the lamp and relay connected to its collector.

The lamps (**LOW C, HIGH C,** and **HIGH D**) provide a visual indication of a NO GO (out-of-tolerance) comparison. The relays (K803, K802, and K804) provide contact closures to drive external sorting equipment.

4.9.2 GO, IN-TOLERANCE

The borrow signals (**ZBO, BO,** and **BOS**; ignore ZBOS for the moment) are connected to an or-gate in the base of Q301. Q301 is normally biased off by R302 which places Q301 collector at a 1-level and turns on Q303. Q303 drives the **GO** lamp which is, therefore, normally on.

If any borrow input is 1, however, it turns on Q301 which turns off Q303 and extinguishes the GO lamp.

4.9.3 CK, PRINT IN-TOLERANCE

When Q301 is off (comparison is **GO** or in-tolerance), its collector is 0 which turns on Q302 and sets **CK** to 1. The CK signal is connected to the PRINT IN-TOLERANCE ONLY position of the DATA READY COMMAND CONTROL, S903 on the rear of the instrument, and enables the print command flip-flop on the program board (paragraph 4.3.3) to issue a **PRT** print command when the comparison result is GO.

4.9.4 CKK, PRINT OUT-OF-TOLERANCE

When Q301 is on (comparison is **NO GO** or out-of-tolerance), its collector is 1 which turns off Q302. When Q302 is off, Q304 is off which sets **CKK** to 1. The CKK signal is connected to the PRINT OUT-OF-TOLERANCE position of the DATA READY COMMAND CONTROL, S903 on the rear of the instrument, and enables the print command flip-flop on the program board (paragraph 4.3.3) to issue a **PRT** print command when the comparison result is NO GO.

4.9.5 LPGP, LAMP ENABLE

The negative return for all of the driver transistors is provided by Q307. Q307 is driven by Q306 which is driven by the **LPGP** signal from the start Schmitt on the program board (paragraph 4.3.1).

4.9.6 LOW D

Although the relay driver board contains a relay driver (Q310) for LOW D measurements, the relay board does not contain a LOW D relay nor does a LOW D lamp exist on the front panel. Also, no LIMIT switches are provided for LOW D. Provision has been made for this circuitry however and connections have been made to the rear-mounted sockets.

4.10 POWER SUPPLY

Diagram V. The power supply provides three regulated voltages (+6V, -15V, and -21V) and a regulated floating ground reference (VREF).

4.10.1 OPERATION

Since the operation of most of the circuits is similar, only the VREF circuit will be described. A full-wave rectifier supplies an unregulated dc voltage to the collector of the series regulator, Q51, whose emitter provides the regulated output, VREF. The VREF output is divided down by R503 and R504 and applied to an error amplifier, Q504 which, through an emitter follower (Q503) controls the conduction of the series regulator to maintain a constant VREF output.

For example, if VREF should go up (further positive from -15V), Q504 base would go up and cause Q504 to conduct more. Q504 collector would go down which would bring Q503 base down and cause Q503 to conduct less. Q503 emitter would go down which would bring Q51 base down and cause Q51 to conduct less. Since Q51 would conduct less, the voltage drop across it would increase and bring the VREF output back down.

The +6-V and -15-V supplies are similar except an emitter follower is not used after the error amplifier. The -21-V output is obtained by a 6-volt zener from the -15-V supply.

CAUTION: Turn off power before removing or replacing etched boards.

CAUTION: Do not operate the instrument on its side unless the relay board is removed.
The relay board contains mercury relays which will not operate properly when the instrument is in other than a horizontal position.

5.1 WARRANTY

We warrant that each new instrument manufactured and sold by us is free from defects in material and workmanship, and that, properly used, it will perform in full accordance with applicable specifications for a period of two years after original shipment. Any instrument or component that is found within the two-year period not to meet these standards after examination by our factory, Sales Engineering Office, or authorized repair agency personnel, will be repaired, or, at our option, replaced without charge, except for tubes or batteries that have given normal service.

5.2 SERVICE

The two-year warranty stated above attests the quality of materials and workmanship in our products. When difficulties do occur, our service engineers will assist in any way possible. If the difficulty cannot be eliminated by use of the following service instructions, please write or phone our Service Department (see rear cover), giving full information of the trouble and of steps taken to remedy it. Be sure to mention the serial and type numbers of the instrument.

Before returning an instrument to General Radio for service, please write to our Service Department or nearest Sales Engineering Office, requesting a "Returned Material Tag." Use of this tag will ensure proper handling and identification. For instruments not covered by the warranty, a purchase order should be forwarded to avoid unnecessary delay.

5.3 ETCHED BOARDS

CAUTION: Turn off power before removing or replacing etched boards.

5.3.1 BOARD EXTENDERS

The instrument features modular construction which greatly simplifies troubleshooting and repair. Most of the circuitry is mounted on plug-in etched boards which can be raised above the instrument by means of board extenders for access to components and test points. Two 24-pin board extenders are required, part number 4215-2024 each. These will accomodate all boards except the power supply board.

In order to use the board extenders, the Nylon polarizing keys in the sockets of the comparator must be removed and the extenders must be installed so that the arrows labeled "front" point to the right-hand side of the instrument as viewed from the front.

5.3.2 REPAIR AND REPLACEMENT

For minimum down-time, a defective board can be replaced immediately and thus keep the instrument on-line while the defective unit is being repaired. Defective boards may be repaired in your facility or sent to the nearest General Radio Repair Center (see rear cover) for repair or replacement. The instrument contains the following plug-in etched boards:

PLUG-IN BOARD	PART NUMBER	POSITION	SOCKETS	REMARKS
Format	1781-4710		SO12, SO13	
Subtractor	1781-4720		SO14, SO15	
Relay Driver	1781-4730		SO17	
Relay	1781-4780		SO27	
Program	1781-4740		SO18, SO19	
Ring-of-Twelve	1781-4760		SO20, SO21	
Parallel-Serial	1781-4770	front	SO22, SO23	
Parallel-Serial	1781-4770	rear	SO24, SO25	
Power Supply	1771-4750		SO11	Adjustment recommended, see 5.4.2

Diagram AG. For additional signal characteristics, see paragraph 6.2 Signal Index. For minimum performance test, see paragraph 3.1.2 Operational Checks.

5.4.1 PRELIMINARY

Introduction. This procedure can be used for troubleshooting or calibration. In either case, the steps should be performed in the order given because one step serves as a foundation for the next.

Troubleshooting. These steps should localize most troubles to a particular board and, in some cases, to a specific circuit. Defective boards may be repaired in your facility or sent to the nearest General Radio Repair Center (see rear of book) for repair or replacement.

When a board is indicated as defective, the trouble can also be the socket connections to the board (the board is not seated properly in the socket or the socket contacts are dirty or misaligned). If a board is intermittent or if a replacement board fails to work, remove the board then reinsert it.

When a transistor is indicated as defective, the trouble can also be the components or wiring associated with the transistor.

Calibration. The Type 1781 Digital Limit Comparator incorporates the high reliability inherent in conservatively-designed, solid-state, digital circuitry and routine calibrations are unnecessary.

Equipment required. The specifications given are those necessary for troubleshooting or calibration of the comparator and are not necessarily those of the suggested equipment.

Autotransformer – Output: 105 to 125V, 10W
Meter: ±3% accuracy
The Type W5M73W Metered Variac Autotransformer is suggested.

Voltmeter – – – – Range: 0 to 25V, dc
Impedance: 20,000 ohms per volt, min
The Type 1806 Electronic Voltmeter is suggested.

Oscilloscope – Bandwidth: 10MHz, min
Sensitivity: 5V/division, min, including probe
Impedance: 10MΩ, min

Pulse – – – – – PRF: 30 Hz
generator Duration: 50ms
Amplitude: -15V, p-to-p
The Type 1398 Pulse Generator or the Type 1217 Unit Pulse Generator with a Type 1201 or Type 1203 Power Supply is suggested.

Data Source – – Digits: 11
Code: 4-bit BCD
Impedance: 47kΩ, max
The Type 1680-A Automatic Capacitance Bridge Assembly is suggested.

Setup. Connect the data source (DATA OUTPUT socket of the Type 1680-A) to the BCD DATA INPUT socket, SO30 on the rear of the comparator.

Use a 2-wire power cord to connect the pulse generator to the ac line. Connect the pulse generator output to SO18 pin 1 (STA) and connect the pulse generator ground to any orange lead in the comparator (VREF).

Note. All signals are measured with respect to VREF (⏚) and *not* chassis ground (CGND⏚). Orange wires are used in the comparator for VREF. Be sure VREF is isolated from chassis ground; use a 2-wire power cord to connect the pulse generator and the oscilloscope to the ac line and don't allow the chassis of the test equipment to touch the chassis of the comparator or the data source.

Remove the relay board. The comparator contains mercury relays which will not operate properly when the instrument is in other than a horizontal position. Since it is necessary to turn the instrument on its side for access to the test points, remove the relay board to prevent possible trouble.

5.4.2 POWER SUPPLY

All of the circuits in the instrument depend on the power supply for proper operation, therefore, it is checked first. The power supply provides four outputs: +6V, VREF, -15V, and -21V.

R510 Set the input line voltage to the comparator to 115V, turn the POWER switch ON, and proceed as follows:

SUPPLY	CONNECT VOLTMETER BETWEEN	ADJUST OR CHECK	FOR
-15V	-15V (SO11-10) and VREF (SO11-6)	R510	14.25 to 15.75V
+6V	+6V (SO11-4) and VREF (SO11-6)	check	5.7 to 6.3V
-21V	-21V (SO11-1) and -15V (SO11-10)	check	5.7 to 6.3V

Set line voltage to 105V and repeat checks; set line voltage to 125V and repeat checks; return line voltage to 115V.

5.4.3 WAVEFORMS

Set the pulse generator for -15-V squarewaves of approximately 50-ms duration at a 30-Hz rate. Trigger the oscilloscope externally on the negative slope of the pulse generator output. Set the data source for range 0, 09999 capacitance, and 09999 loss (on the Type 1680-A, set the MEASUREMENT RATE control to MANUAL, the BALANCE control to HOLD COUNT, and momentarily depress the SET switch to 0, then to 9).

ARC3. Connect the oscilloscope to SO13 pin 8 and check for bursts of 36 pulses; the 0-level must be approximately -15V and the pulses must be 6.9 to 9.5μs in duration with a minimum of 40μs between leading edges.

If continuous pulses instead of bursts: **Program board** 800μs delay or reset ff defective or **format board** ring-of-three defective.

If pulses improper: **Program board** clock generator defective.

If pulses missing: **Pulse generator** output missing or set improperly, or **program board** defective.

ARC12. Connect the oscilloscope to SO21 pin 18 and check for bursts of 12 pulses; the 0-level must be approximately -15V and the pulses must be 6.9 to 9.5μs in duration with a minimum of 120μs between leading edges.

If missing: Check STB signal at SO13-12, if present, **format board** Q106 is defective, if missing **format board** Q101 or ring-of-three is defective.

R12. Connect the oscilloscope to SO21 pin 17 and check reset transition; the 0-level must be approximately -21V and the step must be approximately -1.8V by 200μs.

If missing or improper: Check R12 signal at SO19-3; if missing, check R3 signal at SO19-10; if both missing, **program board** Q414 or Q415 defective. If R3 signal is present but R12 is not, **program board** Q417 is defective. If R12 signal is present, **ring-of-twelve board** is defective.

Input memory data lines. Check each of the four data lines as follows: Connect the oscilloscope to the data line and check for two bursts of four pulses each; the 0-level must be approximately -21V with a minimum duration of 80μs.

If all pulses of a data line are missing: Check RE2 signal at SO25-17 or SO23-17 (as appropriate); if not present, **format board** Q110 is defective; if present, **parallel-serial board** memory ff for that line is defective.

If a pulse is missing: **Data source** line is defective (digit is not set to 9 or bit is missing) or **parallel-serial board** gate (47-k resistor, 470-pF capacitor, and associated diode) for the missing bit is defective.

Borrow outputs. Set the comparator limit switches as follows:

All NO GO lamps (LOW C, HIGH C, and HIGH D/G) must be lit. Connect the oscilloscope to each borrow output; the signals must be as shown in diagram AG.

Set the comparator limit switches as follows:

Only the GO lamp must be lit.

If only high D borrow is missing or improper: **format board** borrow transfer ff or DISSIPATION/CONDUCTANCE UPPER LIMIT switches are defective.

If only low C borrow is missing or improper: **format board** lower converter is defective or CAPACITANCE LOWER LIMIT switches are defective, **subtractor board** lower subtractor is defective or input memory data line outputs from parallel-serial boards are not reaching the subtractor board.

If the high C and high D borrows are missing or improper: **format board** upper converter is defective, **subtractor board** upper subtractor is defective or input memory data line outputs from parallel-serial boards are not reaching the subtractor board.

If all borrows are missing or improper: **format board** Q107 is defective.

If borrows are ok but a NO-GO lamp fails to light: **Relay driver board** driver for that lamp is defective or the **lamp** is defective (four spare lamps are mounted inside the instrument; on top in the right-rear corner).

If borrows are ok but all NO-GO lamps fail to light: **Program board** LPGP signal is defective or **relay driver board** Q306 or Q307 is defective.

If borrows are ok but GO lamp fails to light: **Relay driver board** go nor-gate is defective or the **lamp** is defective (four spare lamps are mounted inside the instrument; on top in the right-rear corner).

PRT. Connect the oscilloscope to SO18 pin 24 and check the PRT print command signal; 0-level must occur at end of the comparison (leading edge of last ARC3 pulse) and must be approximately -15V; 1-level must occur at end of STA signal (pulse generator input).

If missing or improper: **Program board** DATA READY COMMAND CONTROL not set to PRINT ALL or print command ff is defective.

Parts and Diagrams

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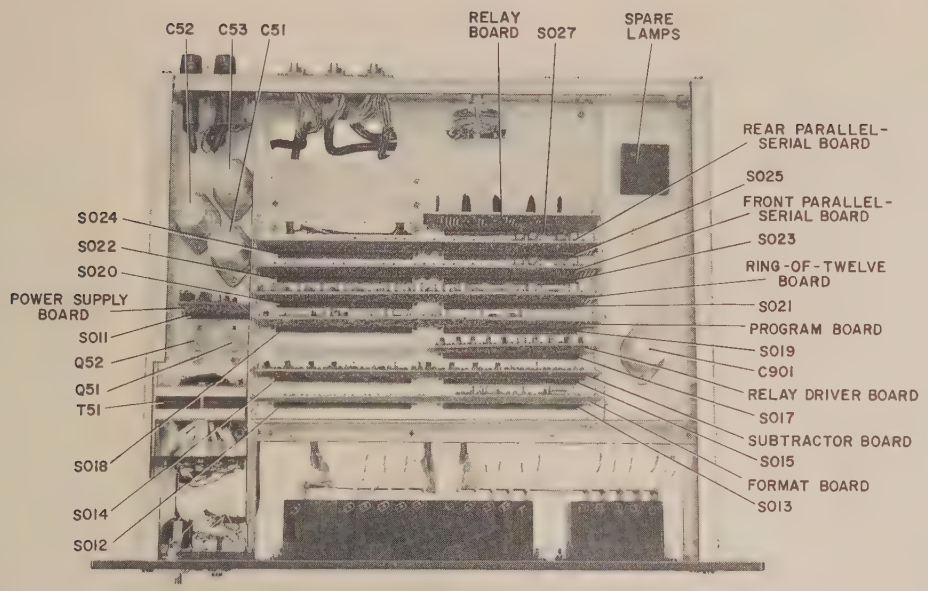
C52
C53
C51
RELAY BOARD
S027
SPARE LAMPS
REAR PARALLEL-SERIAL BOARD
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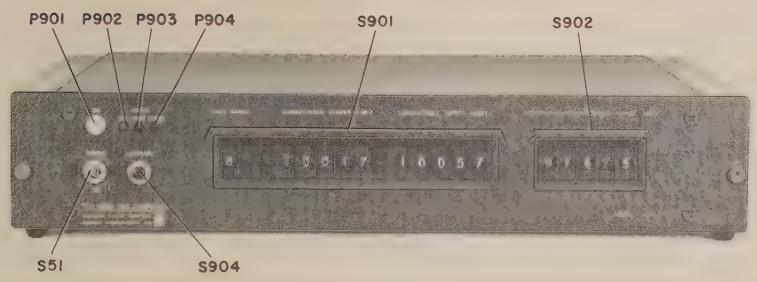
P901
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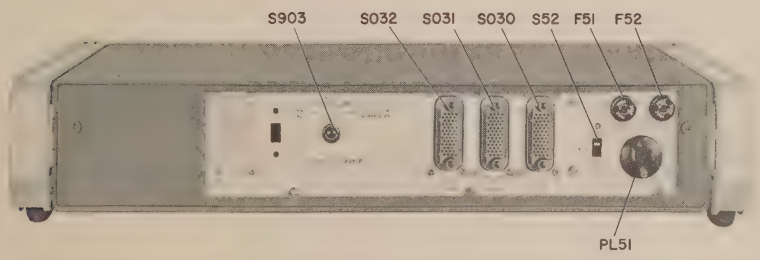
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SIGNAL INDEX

SIGNAL	DESCRIPTION	*CHARACTERISTICS	SOURCE OR MAJOR USE		REAR SOCKET
	NAME OR FUNCTION	*TRUE LEVELS*	*DIAGRAM*	*PRINCIPLES PARAGRAPH*	*CONNECTION*
A	Unregulated +6V	dc, +9V 250mv p-to-p 120Hz ripple	V	4.10	
AA	1st loss digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.6.2, see 4.8.2	
AA1	1st loss digit upper limit transfer	p, +11V, -21V, .3μs, 35μs. 160μs	I	4.7.3, see 4.8.2	
AA2	Not used		I		
AA3	Not used		I		
ARC3	Clock pulses	p, -12V, -2V, .1μs, 1μs, 8μs	I	4.3.2	
ARC12	Ring-of-twelve drive	p, -15V, 0V, .2μs, 1μs, 8μs	H	4.4	
A1	1st loss digit input 1-bit	dc	J	4.6.1, see 4.8.2	SO30-A10, SO32-A10
A2	1st loss digit input 2-bit	dc	J	4.6.1, see 4.8.2	SO30-C10, SO32-C10
A3	1st loss digit input 4-bit	dc	J	4.6.1, see 4.8.2	SO30-E10, SO32-E10
A4	1st loss digit input 2^1- or 8-bit	dc	J	4.6.1, see 4.8.2	SO30-G10, SO32-G10
B	VREF error signal	dc, +.6V	V	4.10	
BB	2nd loss digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.6.4, see 4.8.2	
BB1	2nd loss digit upper limit transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.7.5, see 4.8.2	
BO	High C borrow	p, -15V, +15V	K	4.8.2	
BOB	High C borrow	p, -15V, +15V	K	see 4.8.2	SO31-B9
BOC	High C borrow complement (not used)	p,	K	see 4.8.2	
BOS	High D borrow	p, -13V, +13V	K	4.8.2	
BOSB	High D borrow	p, -13V, +13V	K	see 4.8.2	SO31-D9
BOSC	High D borrow complement (not used)	p	K	see 4.8.2	
B1	2nd loss digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B9, SO32-B9
B2	2nd loss digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D9, SO32-D9
B3	2nd loss digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F9, SO32-F9
B4	2nd loss digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H9, SO32-H9
C	Unregulated -15V	dc, 12V, .6V p-to-p 120Hz ripple	V	4.10	
CC	3rd loss digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.6.4, see 4.8.2	
CGND	Chassis ground			4.10	SO30-H13, SO31-H13, SO32-H13
CK	Out-of-tolerance comparison result	p, -21V, +21V	L	4.3.3, 4.9.1	SO32-E12
CK-CKK	Print command input	p,	G	4.3.3	
CKK	In tolerance comparison result	p, -15V, +15V	L	4.3.3, 4.9.1	
CC1	3rd loss digit upper limit transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.7.5, see 4.8.2	
C1	3rd loss digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-A8, SO32-A8
C2	3rd loss digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-C8, SO32-C8
C3	3rd loss digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-E8, SO32-E8
C4	3rd loss digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-G8, SO32-G8
D	Unregulated VREF	dc, +8V, 1.2V p-to-p 120Hz ripple	V	4.10	
DD	4th loss digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.6.2, see 4.8.2	
DD1	4th loss digit upper limit transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.7.3, see 4.8.2	
D1	4th loss digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B7, SO32-B7
D2	4th loss digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D7, SO32-D7
D3	4th loss digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F7, SO32-F7
D4	4th loss digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H7, SO32-H7
EE	5th loss digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.6.2, see 4.8.2	
EE1	5th loss digit upper limit transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.7.3, see 4.8.2	
EM2	Ring-of-twelve common emitter bus	dc, -1.2V	I	4.5, see 4.4	
EMIT2	Ring-of-twelve common emitter bus	p	I	4.5, see 4.4.2	
E1	5th loss digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-A6, SO32-A6
E2	5th loss digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-C6, SO32-C6
E3	5th loss digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-E6, SO32-E6
E4	5th loss digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-G6, SO32-G6
FF	Loss-to-capacitance shift	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.8.2	
FF1	Loss-to-capacitance shift	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.8.2	
FF3	Loss-to-capacitance shift, enable for STB and RE3	p, +11V, -21V, .3μs, 35μs, 160μs	I	4.8.2	
F1	Loss-to-capacitance shift, connected to -15V	dc, -15V	J	4.8.2	
F2	Loss-to-capacitance shift, connected to -15V	dc, -15V	J	4.8.2	
F3	Loss-to-capacitance shift, connected to -15V	dc, -15V	J	4.8.2	
F4	Loss-to-capacitance shift, connected to -15V	dc, -15V	J	4.8.2	
G	-15-V error signal		V	4.10	
GC	GO-relay common contact		L	4.9.2	SO31-B5
GG	1st capacitance digit input transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.6.2, see 4.8.2	
GOL	GO-lamp drive	dc, -10V	L	4.9.2	
GONC	GO-relay normally-closed contact		L	4.9.2	SO31-D3
GOND	GO-relay normally-open contact		L	4.9.2	SO31-B3
GOR	GO-relay drive	dc, -15V	L	4.9.2	
GG1	1st capacitance digit upper limit transfer	p, +11V, -21V, .3μs, 35μs, 160μs	I	see 4.7.3, see 4.8.2	

SIGNAL	DESCRIPTION	*CHARACTERISTICS	SOURCE OR MAJOR USE		REAR SOCKET
	NAME OR FUNCTION	*TRUE LEVELS*	*DIAGRAM*	*PRINCIPLES PARAGRAPH*	*CONNECTION*
GG2	1st capacitance digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
G1	1st capacitance digit input, 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B5, SO32-B5
G2	1st capacitance digit input, 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D5, SO32-D5
G3	1st capacitance digit input, 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F5, SO32-F5
G4	1st capacitance digit input, 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H5, SO32-H5
HC	HIGH C - relay common contact		L	4.9.1	SO31-D5
HDC	HIGH D - relay common contact		L	4.9.1	SO31-H5
HH	2nd capacitance digit input transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.6.2, see 4.8.2	
HICL	HIGH C - lamp drive	dc, -10V	L	4.9.1	
HICNC	HIGH C - relay normally-closed contact		L	4.9.1	SO31-G2
HICNO	HIGH C - relay normally-open contact		L	4.9.1	SO31-E2
HICR	HIGH C - relay drive	dc, -15V	L	4.9.1	
HIDL	HIGH D - lamp drive	dc, -10V	L	4.9.1	
HIDNC	HIGH D - relay normally-closed contact		L	4.9.1	SO31-H1
HIDNO	HIGH D - relay normally-open contact		L	4.9.1	SO31-F1
HIDR	HIGH D - relay drive	dc, -15V	L	4.9.1	
HH1	2nd capacitance digit upper limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.7.3, see 4.8.2	
HH2	2nd capacitance digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
H1	2nd capacitance digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-A4, SO32-A4
H2	2nd capacitance digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-C4, SO32-C4
H3	2nd capacitance digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-E4, SO32-E4
H4	2nd capacitance digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-G4, SO32-G4
II	3rd capacitance digit input transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.6.2, see 4.8.2	
INH	Balance inhibit		AX		SO30-G12, SO32-G12
II1	3rd capacitance digit upper limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.7.3, see 4.8.2	
II2	3rd capacitance digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
I1	3rd capacitance digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B3, SO32-B3
I2	3rd capacitance digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D3, SO32-D3
I3	3rd capacitance digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F3, SO32-F3
I4	3rd capacitance digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H3, SO32-H3
JJ	4th capacitance digit input transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.6.2, see 4.8.2	
JJ1	4th capacitance digit upper limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.7.3, see 4.8.2	
JJ2	4th capacitance digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
J1	4th capacitance digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-A2, SO32-A2
J2	4th capacitance digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-C2, SO32-C2
J3	4th capacitance digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-E2, SO32-E2
J4	4th capacitance digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-G2, SO32-G2
KK	5th capacitance digit input transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.6.2, see 4.8.2	
KK1	5th capacitance digit upper limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.7.3, see 4.8.2	
KK2	5th capacitance digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
K1	5th capacitance digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B1, SO32-B1
K2	5th capacitance digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D1, SO32-D1
K3	5th capacitance digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F1, SO32-F1
K4	5th capacitance digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H1, SO32-H1
LC	LOW C - relay common contact		L	4.9.1	SO31-F5
LDC	LOW D - relay common contact (provision only)		L	4.9.1	SO31-A6
LL	Range digit input transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.6.2, see 4.8.2	
LOCL	LOW C - lamp drive		L	4.9.1	
LOCNC	LOW C - relay normally-closed contact		L	4.9.1	SO31-C2
LOCNO	LOW C - relay normally-open contact		L	4.9.1	SO31-A2
LOCR	LOW C - relay drive	dc, -15V	L	4.9.1	
LODL	LOW D - lamp drive (lamp not installed)		L	4.9.6	
LODNC	LOW D - relay normally-closed contact (provision only)		L	4.9.6	SO31-D1
LODNO	LOW D - relay normally-open contact (provision only)		L	4.9.6	SO31-B1
LODR	LOW D - relay drive (relay not installed)		L	4.9.6	
LPGP	Relay driver common		G	4.3.1	
LL1	Range digit upper limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	see 4.7.3, see 4.8.2	
LL2	Range digit lower limit transfer	p, +11V, -21V, .3µs, 35µs, 160µs	I	4.8.2	
L1	Range digit input 1-bit	dc	J	see 4.6.1, see 4.8.2	SO30-B11, SO32-B11
L2	Range digit input 2-bit	dc	J	see 4.6.1, see 4.8.2	SO30-D11, SO32-D11
L3	Range digit input 4-bit	dc	J	see 4.6.1, see 4.8.2	SO30-F11, SO32-F11
L4	Range digit input 2^1- or 8-bit	dc	J	see 4.6.1, see 4.8.2	SO30-H11, SO32-H11
PRT	Print command		G	4.3.3	SO31-C4, SO32-A12
R	Not used				
RE1	Reset, enable for clock generator	p, -13V, +13V	G	4.3.2	

SIGNAL	DESCRIPTION	*CHARACTERISTICS	SOURCE OR MAJOR USE		REAR SOCKET
	NAME OR FUNCTION	*TRUE LEVELS*	*DIAGRAM*	*PRINCIPLES PARAGRAPH*	*CONNECTION*
RE2	Reset, clear memories	p, +12V, -19V, .2μs, 20μs, 55μs	H	4.4, 4.6.3	
RE2L	Reset, RE1 to 0		G	4.3.3	
RG	Not used				
RG2	Not used				
R3	Set ring-of-three to RE2	p	G	4.3.1	
R12	Set ring-of-twelve to L	p	G	4.3.1	
STA	Compare enable and initiate	dc	G	4.3.1	SO30-A12, SO31-A4
STAB	Compare initiate	dc	G	4.3.4	SO31-E4
STA1	Reset, RE1 to 0	p	G	4.3.5	
STA2	Reset, RE1 to 1	p	G	4.3.2	
STA3	Reset, PRT to 1	p	G	4.3.3	
STB	High and low C store borrow	p, +12V, -20V, .2μs, 20μs, 55μs	H	4.4, see 4.8.2	
STBD	High and low D store borrow	p, -13V, +13V, .2μs, 2μs, 30μs	H	4.8.2	
U1C	Upper limit 1-bit complement		H	4.7.3	
U2	Upper limit 2-bit	p	H	4.7.3	
U4C	Upper limit 4-bit complement	p	H	4.7.3	
U8	Upper limit 2^1- or 8-bit complement	p	H	4.7.3	
VREF	Floating ground	p	V	4.10	SO30-C12, SO31-C12, SO32-C12
X1	Input 1-bit	p, -15V, +15V	J	4.6.2	
X2C	Input 2-bit complement	p, -15V, +15V	J	see 4.6.2, 4.8.1	
X4	Input 4-bit	p, -15V, +15V	J	see 4.6.2	
X8C	Input 2^1- or 8-bit complement	p, -15V, +15V	J	see 4.6.2, 4.8.1	
ZBO	Low C borrow	p, -15V, +15V	K	4.8.2	
ZBOB	Low C borrow	p, -15V, +15V	K	see 4.8.2	SO31-F9
ZBOC	Low C borrow complement (not used)	p	K	see 4.8.2	
ZBOS	Low D borrow (not used)	p	K	see 4.8.2	
ZBOSB	Low D borrow (not used)	p	K	see 4.8.2	
ZBOSC	Low D borrow complement (not used)	p	K	see 4.8.2	SO31-H9
ZL1	Lower limit 1-bit	p	H	see 4.7.3	
ZL2C	Lower limit 2-bit complement	p	H	see 4.7.3	
ZL4	Lower limit 4-bit	p	H	see 4.7.3	
ZL8C	Lower limit 2^1- or 8-bit complement	p	H	see 4.7.3	
ZX1C	Input 1-bit complement	p, -15V, +15V	J	see 4.6.2, 4.8.1	
ZX2	Input 2-bit	p, -15V, +15V	J	4.6.2	
ZX4C	Input 4-bit complement	p, -15V, +15V	J	see 4.6.2, 4.8.1	
ZX8	Input 2^1- or 8-bit	p, -15V, +15V	J	4.6.2	
OLL	Lower limit decimal 0	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
1LL	Lower limit decimal 1	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
2LL	Lower limit decimal 2	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
3LL	Lower limit decimal 3	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
4LL	Lower limit decimal 4	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
5LL	Lower limit decimal 5	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
6LL	Lower limit decimal 6	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
7LL	Lower limit decimal 7	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
8LL	Lower limit decimal 8	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
9LL	Lower limit decimal 9	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
0UL	Upper limit decimal 0	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
1UL	Upper limit decimal 1	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
2UL	Upper limit decimal 2	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
3UL	Upper limit decimal 3	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
4UL	Upper limit decimal 4	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
5UL	Upper limit decimal 5	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
6UL	Upper limit decimal 6	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
7UL	Upper limit decimal 7	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
8UL	Upper limit decimal 8	p. +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
9UL	Upper limit decimal 9	p, +11V, -21V, .3μs, 35μs, 160μs	H	see 4.7.2	
+6V	Supply voltage	dc, +6V, 10mv p-to-p 120Hz ripple	V	4.10	SO31-A12
-15V	Supply voltage	dc, -15V, 10mv p-to-p 120Hz ripple	V	4.10	SO31-G12
-21V	Supply voltage	dc, -21V, 10mv p-to-p 120Hz ripple	V	410	SO31-E12

* Signal type (p = pulse), baseline, amplitude, risetime, falltime, duration.

PARTS LIST

CAPACITORS

C51	Electrolytic, 600X600µF +100-10% 15V	4450-5622
C52	Electrolytic, 400X400µF +100-10% 25V	4450-5621
C53	Electrolytic, 600X600µF +100-10% 15V	4450-5622
C101	Ceramic, 0.0022µF ±20% 500V	4404-2220
C102	Ceramic, 330pF -10% 500V	4404-1338
C103	Ceramic, 0.0022µF ±20% 500V	4404-2220
C104	Ceramic, 0.02µF +80-20% 50V	4402-3200
C105	Ceramic, 0.0022µF ±20% 500V	4404-2220
C106	Ceramic, 330pF ±10% 500V	4404-1338
C107	Ceramic, 0.001µF ±10% 500V	4405-2108
C201 thru C212	Ceramic, 330pF ±10% 500V	4404-1338
C401	Ceramic, 330pF ±10% 500V	4404-1338
C402	Ceramic, 330pF ±10% 500V	4404-1338
C403	Plastic, 0.033pF ±10% 100V	4860-7865
C404	Ceramic, 330pF ±10% 500V	4404-1338
C405	Plastic, 0.015µF ±10% 100V	4860-7655
C406 thru C410	Ceramic, 330pF ±10% 500V	4404-1338
C411	Ceramic, 0.22µF ±20% 25V	4400-2052
C412	Ceramic, 330pF ±10% 500V	4404-1338
C413	Plastic, 0.022µF ±10% 100V	4860-7860
C501	Ceramic, 0.1µF +80-20% 50V	4403-4100
C601 thru C611	Ceramic, 0.0022µF ±20% 500V	4404-2220
C612	Ceramic, 0.02µF +80-20% 50V	4402-3200
C613	Ceramic, 0.0022µF ±20% 500V	4404-2220
C701 thru C724	Ceramic, 470pF ±10% 500V	4404-1478
C725 thru C728	Ceramic, 330pF ±10% 500V	4404-1338
C801 thru C808	Ceramic, 0.0047µF ±10% 500V	4407-2478
C901	Electrolytic, 400X400µF +100-10% 25V	4450-5621

DIODES

CR51	Type IN645	6082-1016
CR52	Type IN645	6082-1016
CR53 thru CR58	Type IN3253	6081-1001
CR101 thru CR143	Type IN4009	6082-1012
CR201	Type IN645	6082-1016
CR202	Type IN4009	6082-1012
CR203	Type IN4009	6082-1012
CR204	Type IN4009	6082-1012
CR205 thru CR208	Type IN645	6082-1016
CR209	Type IN4009	6082-1012
CR210	Type IN4009	6082-1012
CR211	Type IN4009	6082-1012
CR212	Type IN645	6082-1016
CR213	Type IN4009	6082-1012
CR214	Type IN4009	6082-1012
CR215	Type IN4009	6082-1012

DIODES (cont)

CR216 thru CR219	Type IN645	6082-1016
CR220	Type IN4009	6082-1012
CR221	Type IN4009	6082-1012
CR222	Type IN4009	6082-1012
CR301 thru CR310	Type IN645	6082-1016
CR401 thru CR411	Type IN4009	6082-1012
CR501	Type IN4009	6082-1012
CR502	Type IN746	6083-1005
CR601 thru CR626	Type IN4009	6082-1012
CR701 thru CR728	Type IN3604	6082-1001
CR729 thru CR732	Type IN645	6082-1016

FUSES

F51	0.5A 3AG Slo-Blo	5330-1000
F52	0.25A 3AG Slo-Blo	5330-0700

RELAYS

K801 thru K804	Mercury wetted spdt C.P. Clare HGSM5011	6090-1040

LAMPS

P901	Number 1465, 14V, 65mA, uses 7510-2410 socket	GO 5600-0311
P902	Number 1465, 14V 65mA, uses 7510-2400 socket	LOW C 5600-0311
P903	Number 1465, 14V 65mA, uses 7510-2400 socket	HIGH C 5600-0311
P904	Number 1465, 14V 65mA, uses 7510-2400 socket	HIGH D/G 5600-0311
Spare lamps	Four spare lamps are mounted inside the instrument; on top in the right-rear corner.	

PLUGS

PL51	3-terminal power plug, consists of:	
	2-terminal power plug	4240-0600
	Ground pin	4240-0800

TRANSISTORS

Q51	Type 40250	8210-1095
Q52	Type 40250	8210-1095
Q101	Type 2N1304	8210-1304
Q102	Type 2N1304	8210-1304
Q103	Type 2N1305	8210-1305
Q104	Type 2N1305	8210-1305
Q105	Type 2N1304	8210-1304
Q106	Type 2N1305	8210-1305
Q107	Type 2N1304	8210-1304
Q108	Type 2N1304	8210-1304

TRANSISTORS (cont)

Q109	Type 2N1305	8210-1305
Q110	Type 2N1304	8210-1304
Q111	Type 2N1305	8210-1305
Q112	Type 2N1305	8210-1305
Q201	Type 2N3414	8210-1047
Q202 thru Q205	Type 2N1305	8210-1305
Q206 thru Q209	Type 2N3414	8210-1047
Q210 thru Q213	Type 2N1305	8210-1305
Q214	Type 2N3414	8210-1047
Q215	Type 2N3414	8210-1047
Q216	Type 2N3414	8210-1047
Q301	Type 2N3414	8210-1047
Q302	Type 2N1305	8210-1305
Q303 thru Q310	Type 2N3414	8210-1047
Q401	Type 2N3414	8210-1047
Q402 thru Q409	Type eN1305	8210-1047
Q410	Type 2N1304	8210-1304
Q411	Type 2N1304	8210-1304
Q412	Type 2N3414	8210-1047
Q413	Type 2N1305	8210-1305
Q414	Type 2N1304	8210-1304
Q415	Type 2N1305	8210-1305
Q416	Type 2N3638	8210-1096
Q417	Type 2N3638	8210-1096
Q501	Type 2N697	8210-1040
Q502	Type 2N3414	8210-1047
Q503	Type 2N3414	8210-1047
Q504	Type 2N3414	8210-1047
Q505	Type 2N3414	8210-1047
Q601	Type 2N1304	8210-1304
Q602	Type 2N1304	8210-1304
Q603	Type 2N1305	8210-1305
Q604	Type 2N1304	8210-1304
Q605	Type 2N1305	8210-1305
Q606	Type 2N1304	8210-1304
Q607	Type 2N1305	8210-1305
Q608	Type 2N1304	8210-1304
Q609	Type 2N1305	8210-1305
Q610	Type 2N1304	8210-1304
Q611	Type 2N1305	8210-1305
Q612	Type 2N1304	8210-1304
Q613	Type 2N1305	8210-1305
Q614	Type 2N1304	8210-1304
Q615	Type 2N1305	8210-1305
Q616	Type 2N1304	8210-1304
Q617	Type 2N1305	8210-1305
Q618	Type 2N1304	8210-1304
Q619	Type 2N1305	8210-1305
Q620	Type 2N1304	8210-1304
Q621	Type 2N1305	8210-1305
Q622	Type 2N1304	8210-1304
Q623	Type 2N1305	8210-1305
Q624	Type 2N1304	8210-1304
Q625	Type 2N1305	8210-1305
Q701 thru Q704	Type 2N1305	8210-1305

RESISTORS

R101 thru R104	Composition, 10kΩ ±5% 1/2W	6100-3105
R105	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R106	Composition, 1.5kΩ ±5% 1/2W	6100-2155
R107	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R108	Composition, 39kΩ ±5% 1/2W	6100-3395
R109	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R110	Composition, 1.5kΩ ±5% 1/2W	6100-2155
R111	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R112	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R113	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R114	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R115	Composition, 1.5kΩ ±5% 1/2W	6100-2155
R116	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R117	Composition, 47kΩ ±5% 1/2W	6100-3475
R118	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R119	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R120	Composition, 15kΩ ±5% 1/2W	6100-3155
R121	Composition, 12kΩ ±5% 1/2W	6100-3125
R122	Composition, 39kΩ ±5% 1/2W	6100-3395
R123	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R201	Composition, 10kΩ ±5% 1/2W	6100-3105
R202	Composition, 39kΩ ±5% 1/2W	6100-3395
R203	Composition, 39kΩ ±5% 1/2W	6100-3395
R204	Composition, 39kΩ ±5% 1/2W	6100-3395
R205	Composition, 13kΩ ±5% 1/2W	6100-3135
R206	Composition, 10kΩ ±5% 1/2W	6100-3105
R207	Composition, 47kΩ ±5% 1/2W	6100-3475
R208	Composition, 47kΩ ±5% 1/2W	6100-3475
R209	Composition, 47kΩ ±5% 1/2W	6100-3475
R210	Composition, 10kΩ ±5% 1/2W	6100-3105
R211	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R212	Composition, 12kΩ ±5% 1/2W	6100-3125
R213	Composition, 15kΩ ±5% 1/2W	6100-3155
R214	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R215	Composition, 13kΩ ±5% 1/2W	6100-3135
R216	Composition, 12kΩ ±5% 1/2W	6100-3125
R217	Composition, 13kΩ ±5% 1/2W	6100-3135
R218	Composition, 39kΩ ±5% 1/2W	6100-3395
R219	Composition, 39kΩ ±5% 1/2W	6100-3395
R220	Composition, 39kΩ ±5% 1/2W	6100-3395
R221	Composition, 10kΩ ±5% 1/2W	6100-3105
R222	Composition, 39kΩ ±5% 1/2W	6100-3395
R223	Composition, 39kΩ ±5% 1/2W	6100-3395
R224	Composition, 39kΩ ±5% 1/2W	6100-3395
R225	Composition, 12kΩ ±5% 1/2W	6100-3125
R226	Composition, 13kΩ ±5% 1/2W	6100-3135
R227	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R228	Composition, 15kΩ ±5% 1/2W	6100-3155
R229	Composition, 12kΩ ±5% 1/2W	6100-3125
R230	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R231	Composition, 47kΩ ±5% 1/2W	6100-3475
R232	Composition, 13kΩ ±5% 1/2W	6100-3135
R233	Composition, 10kΩ ±5% 1/2W	6100-3105
R234	Composition, 39kΩ ±5% 1/2W	6100-3395
R235	Composition, 39kΩ ±5% 1/2W	6100-3395
R236	Composition, 39kΩ ±5% 1/2W	6100-3395
R237	Composition, 13kΩ ±5% 1/2W	6100-3135
R238	Composition, 22kΩ ±5% 1/2W	6100-3225
R239	Composition, 22kΩ ±5% 1/2W	6100-3225
R240	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R241	Composition, 10kΩ ±5% 1/2W	6100-3105
R242	Composition, 39kΩ ±5% 1/2W	6100-3395
R243	Composition, 39kΩ ±5% 1/2W	6100-3395
R244	Composition, 39kΩ ±5% 1/2W	6100-3395
R245	Composition, 13kΩ ±5% 1/2W	6100-3135
R246	Composition, 10kΩ ±5% 1/2W	6100-3105
R247	Composition, 47kΩ ±5% 1/2W	6100-3475
R248	Composition, 47kΩ ±5% 1/2W	6100-3475

RESISTORS (cont)

R249	Composition, 47kΩ ±5% 1/2W	6100-3475
R250	Composition, 10kΩ ±5% 1/2W	6100-3105
R251	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R252	Composition, 12kΩ ±5% 1/2W	6100-3125
R253	Composition, 15kΩ ±5% 1/2W	6100-3155
R254	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R255	Composition, 13kΩ ±5% 1/2W	6100-3135
R256	Composition, 12kΩ ±5% 1/2W	6100-3125
R257	Composition 13kΩ ±5% 1/2W	6100-3135
R258	Composition, 39kΩ ±5% 1/2W	6100-3395
R259	Composition, 39kΩ ±5% 1/2W	6100-3395
R260	Composition, 39kΩ ±5% 1/2W	6100-3395
R261	Composition, 10kΩ ±5% 1/2W	6100-3105
R262	Composition, 39kΩ ±5% 1/2W	6100-3395
R263	Composition, 39kΩ ±5% 1/2W	6100-3395
R264	Composition, 39kΩ ±5% 1/2W	6100-3395
R265	Composition, 12kΩ ±5% 1/2W	6100-3125
R266	Composition, 13kΩ ±5% 1/2W	6100-3135
R267	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R268	Composition, 15kΩ ±5% 1/2W	6100-3155
R269	Composition, 12kΩ ±5% 1/2W	6100-3125
R270	Composition 1.8kΩ ±5% 1/2W	6100-2185
R271	Composition, 47kΩ ±5% 1/2W	6100-3475
R272	Composition, 13kΩ ±5% 1/2W	6100-3135
R273	Composition, 10kΩ ±5% 1/2W	6100-3105
R274	Composition, 39kΩ ±5% 1/2W	6100-3395
R275	Composition, 39kΩ ±5% 1/2W	6100-3395
R276	Composition, 39kΩ ±5% 1/2W	6100-3395
R277	Composition, 13kΩ ±5% 1/2W	6100-3135
R278	Composition, 22kΩ ±5% 1/2W	6100-3225
R279	Composition, 22kΩ ±5% 1/2W	6100-3225
R280	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R301	Composition, 15kΩ ±5% 1/2W	6100-3155
R302	Composition, 22kΩ ±5% 1/2W	6100-3225
R303	Composition, 1.2kΩ ±5% 1/2W	6100-2125
R304	Composition, 10kΩ ±5% 1/2W	6100-3105
R305	Composition, 10kΩ ±5% 1/2W	6100-3105
R306	Composition, 5.6kΩ ±5% 1/2W	6100-2565
R307	Composition, 27kΩ ±5% 1/2W	6100-3275
R308	Composition, 56kΩ ±5% 1/2W	6100-0565
R309	Composition, 1kΩ ±5% 1/2W	6100-2105
R310	Composition, 5.6kΩ ±5% 1/2W	6100-2565
R311	Composition, 27kΩ ±5% 1/2W	6100-3275
R312	Composition, 1kΩ ±5% 1/2W	6100-2105
R313	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R314	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R315	Composition, 15kΩ ±5% 1/2W	6100-3155
R316	Composition, 100Ω ±5% 1/2W	6100-1105
R317	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R318	Composition, 5.6kΩ ±5% 1/2W	6100-2565
R319	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R320	Composition, 15kΩ ±5% 1/2W	6100-3155
R321	Composition, 100Ω ±5% 1/2W	6100-1105
R322	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R323	Composition, 15kΩ ±5% 1/2W	6100-3155
R324	Composition, 100Ω ±5% 1/2W	6100-1105
R325	Composition, 8.2kΩ ±5% 1/2W	6100-2825
R326	Composition, 15kΩ ±5% 1/2W	6100-3155
R327	Composition, 100Ω ±5% 1/2W	6100-1105
R401	Composition, 220kΩ ±5% 1/2W	6100-4225
R402	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R403	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R404	Composition, 470Ω ±5% 1/2W	6100-1475
R405	Composition, 560Ω ±5% 1/2W	6100-1565
R406	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R407	Composition, 5.6kΩ ±5% 1/2W	6100-2565
R408	Composition, 6.8kΩ ±5% 1/2W	6100-2685
R409	Composition, 1kΩ ±5% 1/2W	6100-2105
R410	Composition, 47kΩ ±5% 1/2W	6100-3475

RESISTORS (cont)

R411	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R412	Composition, 15kΩ ±5% 1/2W	6100-3155
R413	Composition, 39kΩ ±5% 1/2W	6100-3395
R414	Composition, 12kΩ ±5% 1/2W	6100-3125
R415	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R416	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R417	Composition, 12kΩ ±5% 1/2W	6100-3125
R418	Composition, 15kΩ ±5% 1/2W	6100-3155
R419	Composition, 15kΩ ±5% 1/2W	6100-3155
R420	Composition, 12kΩ ±5% 1/2W	6100-3125
R421	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R422	Composition, 1kΩ ±5% 1/2W	6100-2105
R423	Composition, 15kΩ ±5% 1/2W	6100-3155
R424	Composition, 15kΩ ±5% 1/2W	6100-3155
R425	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R426	Composition, 12kΩ ±5% 1/2W	6100-3125
R427	Composition, 12kΩ ±5% 1/2W	6100-3125
R428	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R429	Composition, 22kΩ ±5% 1/2W	6100-3225
R430	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R431	Composition, 39kΩ ±5% 1/2W	6100-3395
R432	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R433	Composition, 10kΩ ±5% 1/2W	6100-3105
R434	Composition, 10kΩ ±5% 1/2W	6100-3105
R435 thru R438	Composition, 47kΩ ±5% 1/2W	6100-3475
R439	Composition, 10kΩ ±5% 1/2W	6100-3105
R440	Composition, 10kΩ ±5% 1/2W	6100-3105
R441	Composition, 82kΩ ±5% 1/2W	6100-3825
R442	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R443	Composition, 120kΩ ±5% 1/2W	6100-4125
R444	Composition, 47kΩ ±5% 1/2W	6100-3475
R445	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R446	Composition, 39kΩ ±5% 1/2W	6100-3395
R447	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R448	Composition, 10kΩ ±5% 1/2W	6100-3105
R449	Composition, 10kΩ ±5% 1/2W	6100-3105
R450	Composition, 10kΩ ±5% 1/2W	6100-3105
R451	Composition, 10kΩ ±5% 1/2W	6100-3105
R501	Film, 4.75K ±10% 1/4W	6350-1475
R502	Film, 13.3K ±1% 1/4W	6350-2133
R503	Film, 111.5K ±1% 1/4W	6350-2115
R504	Film, 5.36K ±1% 1/4W	6350-1536
R505	Composition, 5.1K ±1% 1/4W	6099-2515
R506	Composition, 22K ±1% 1/4W	6099-3225
R507	Composition, 220Ω ±1% 1/4W	6099-1225
R508	Composition, 180Ω ±1% 1/4W	6099-1185
R509	Composition, 330Ω ±1% 1/4W	6099-1335
R510	Potentiometer, wire wound 100Ω ±10%	6059-1109
R511	Composition, 470Ω ±1% 1/4W	6099-1475
R512	Composition, 2.2K ±1% 1/4W	6099-2225
R513	Composition, 300K ±1% 1/4W	6099-4339
R601 thru R604	Composition, 10kΩ ±5% 1/2W	6100-3105
R605	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R606	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R607	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R608	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R609	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R610	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R611	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R612	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R613	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R614	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R615	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R616	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R617	Composition, 3.3kΩ ±5% 1/2W	6100-2335

RESISTORS (cont)

R618	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R619	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R620	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R621	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R622	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R623	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R624	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R625	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R626	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R627	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R628	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R629	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R630	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R631	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R632	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R633	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R634	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R635	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R636	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R637	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R638	Composition, 3.3kΩ ±5% 1/2W	6100-2335
R639	Composition, 1.8kΩ ±5% 1/2W	6100-2185
R640	Composition, 2.7kΩ ±5% 1/2W	6100-2275
R701 thru R728	Composition, 47kΩ ±5% 1/2W	6100-3475
R729 thru R732	Composition, 12kΩ ±5% 1/2W	6100-3125
R733 thru R736	Composition, 13kΩ ±5% 1/2W	6100-3135
R737 thru R740	Composition, 2.2kΩ ±5% 1/2W	6100-2225
R801 thru R808	Composition, 120Ω ±5% 1/2W	6100-1125

SWITCHES

S51	Toggle, dpst, A.H. and H. 83053-SA	POWER	7910-1300

SWITCHES (cont)

S52	Slide, spdt, Muter 4603	line	7910-0831
*S901	Digiswitch 3-G-103	LIMIT RANGE, CAPACITANCE UPPER and LOWER LIMIT	7917-1002
*S902	Digiswitch 3-G-104	DISSIPATION/ CONDUCTANCE UPPER LIMIT	7917-1003
S903	Rotary, single-section, single-pole, three-position	DATA READY COMMAND CONTROL	7890-4390
S904	Push-button, spst momentary, normally open	COMPARE	7870-1511

*Part number listed is for entire assembly. Individual sections are not available from General Radio but can be ordered from the Digitran Company:

LIMIT RANGE section	Digitran 304B
Blank sections	Digitran SP
All other sections	Digitran 331B

SOCKETS

SO11	10-contact, Methode CD-610S	4230-2710
SO12 thru SO27	24-contact, Methode CD-624S	4230-2724
SO30	52-pin socket, Amphenol 220 Series BCD DATA OUTPUT	*
SO31	52-pin socket, Amphenol 220 Series RELAY CONTACTS OUTPUT	*
SO32	52-pin socket, Amphenol 220 Series BCD DATA OUTPUT	*

*Each 52-pin socket consists of:

Socket block	4230-5000
Socket hardware	4230-5001
Male contacts (55)	4230-5003

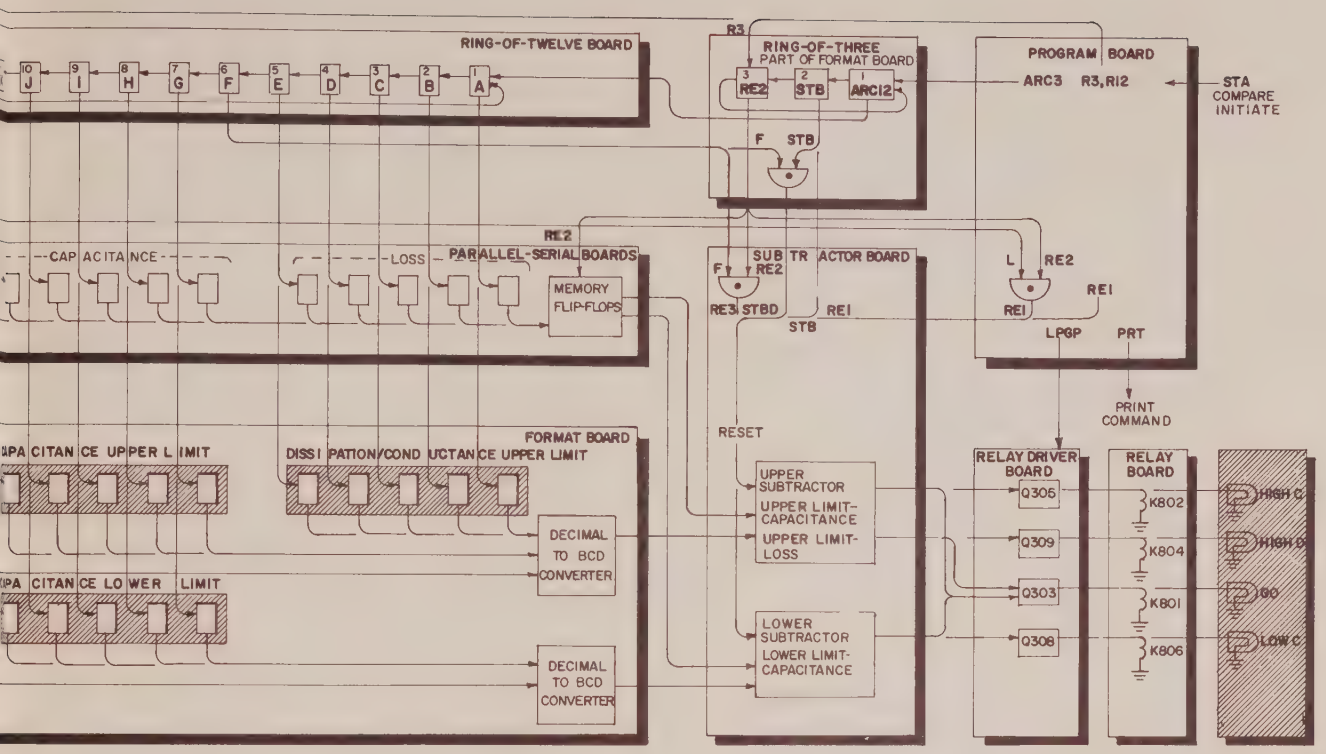
These sockets require special tools for assembly or disassembly:

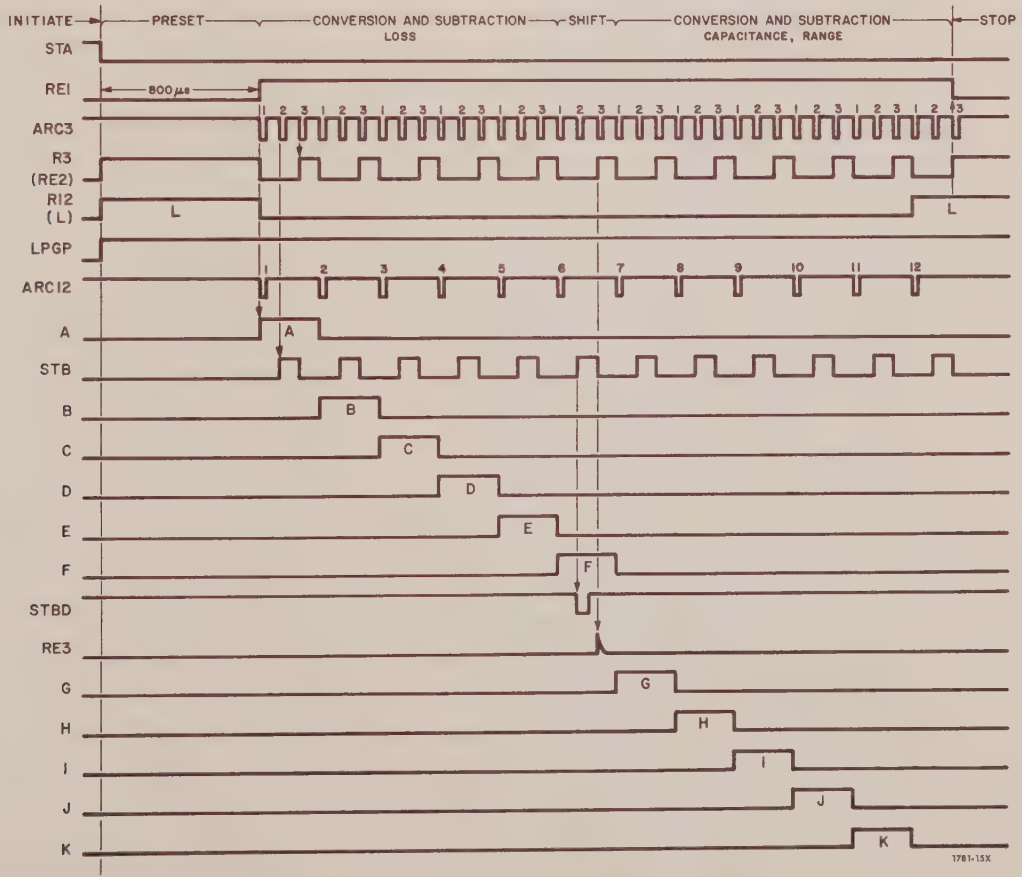
Amphenol crimp tool 294-78 or 294-125
Amphenol insertion tool 294-123
Amphenol removal tool 294-122

TRANSFORMERS

T51	Power transformer	0345-4018

R12
12
L
RANG
RANK
LIM

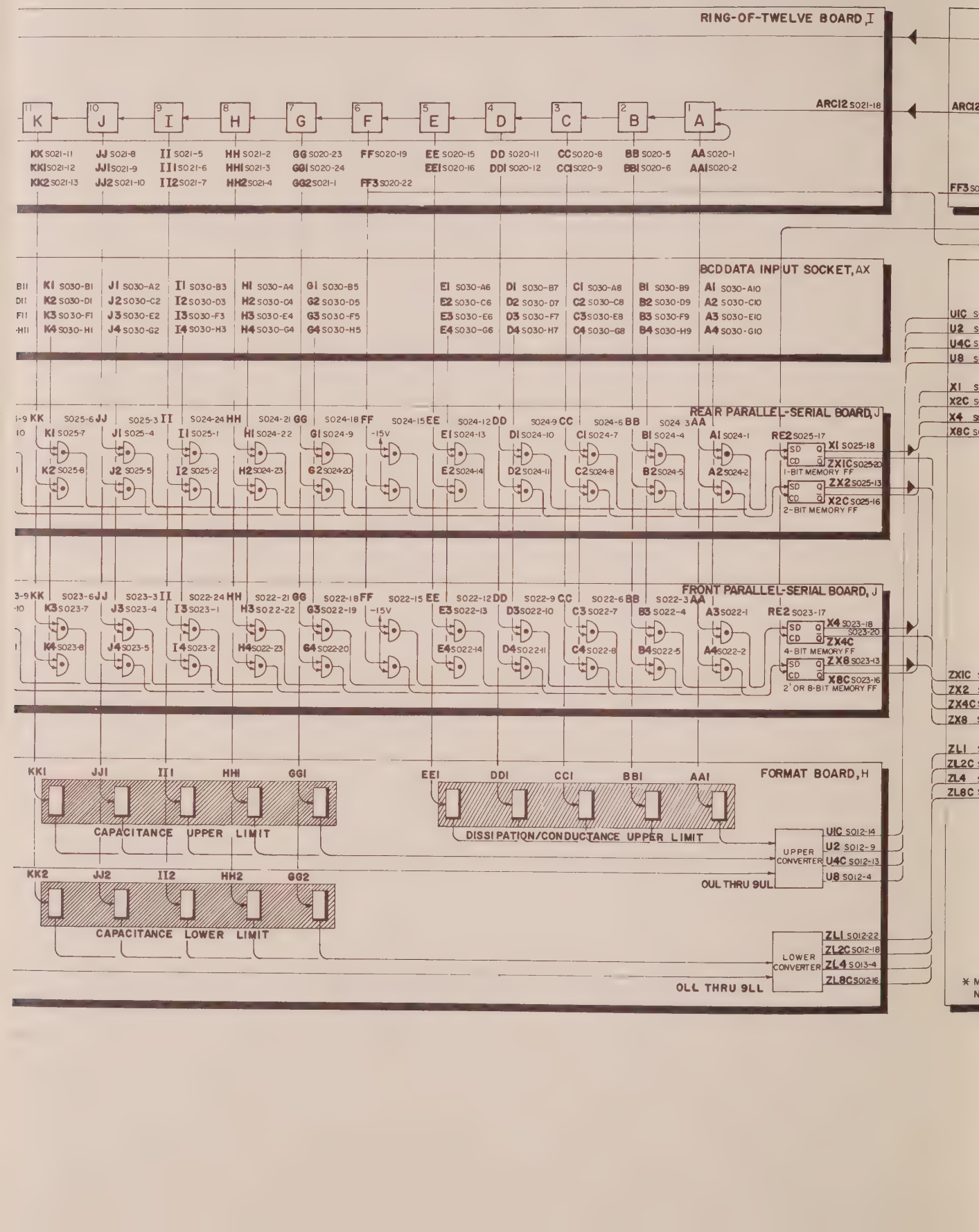

RING-OF-TWELVE BOARD
RING-OF-THREE
PART OF FORMAT BOARD
PROGRAM BOARD
ARC3 R3,RI2
STA
COMPARE
INITIATE
R3
RE2
STB
ARCI2
F STB
RE2
CAPACITANCE
LOSS
PARALLEL-SERIAL BOARDS
MEMORY
FLIP-FLOPS
SUBTRACTOR BOARD
RE3 STBD
REI
STB
L RE2
REI
LPGP PRT
PRINT
COMMAND
RESET
FORMAT BOARD
DISSIPATION/CONDUCTANCE UPPER LIMIT
DECIMAL
TO BCD
CONVERTER
UPPER
SUBTRACTOR
UPPER LIMIT-
CAPACITANCE
UPPER LIMIT-
LOSS
LOWER
SUBTRACTOR
LOWER LIMIT-
CAPACITANCE
RELAY DRIVER
BOARD
Q305
Q309
Q303
Q308
RELAY
BOARD
K802
K804
K801
K806
HIGH C
HIGH D
GO
LOW C

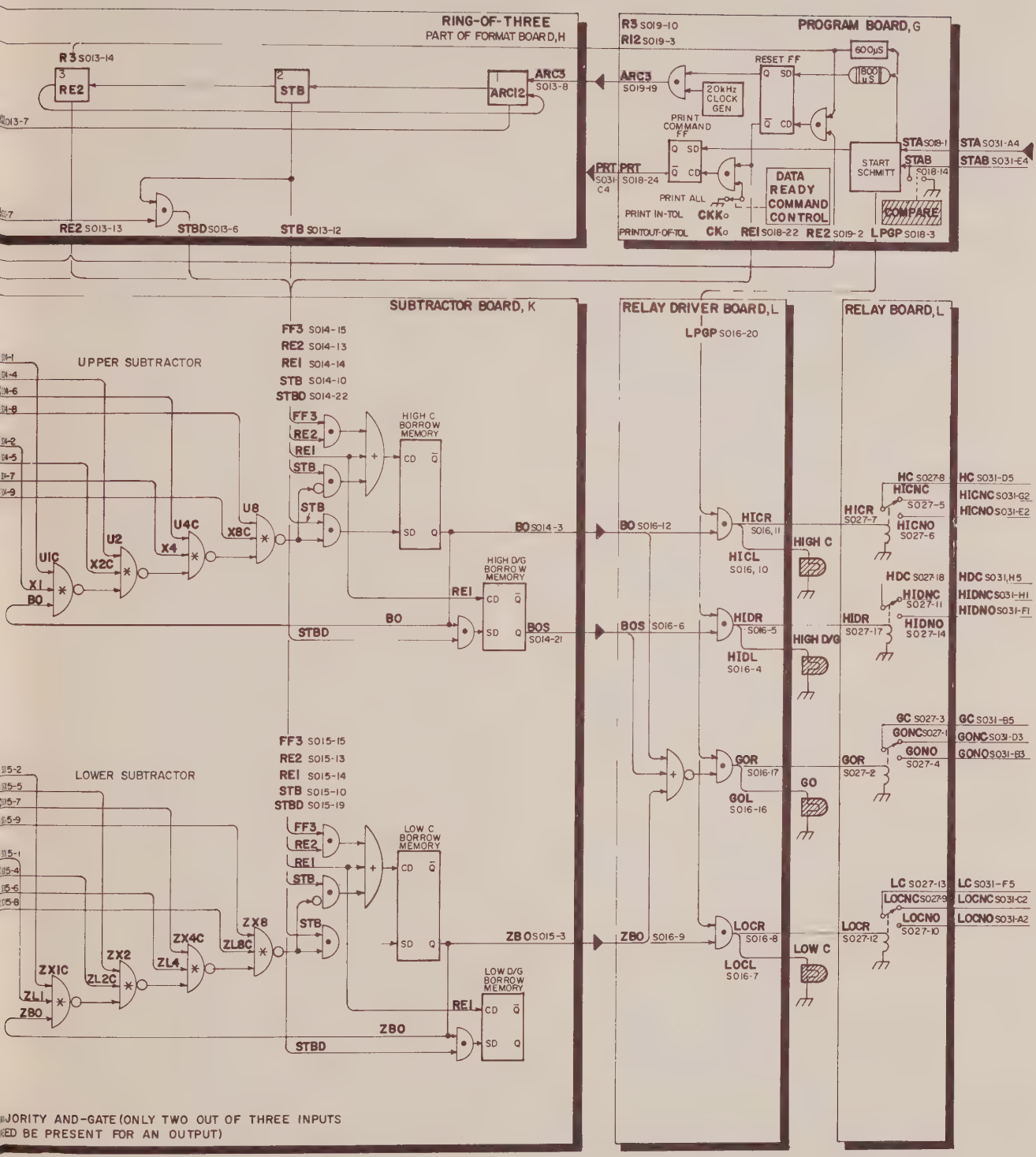

INITIATE
PRESET
CONVERSION AND SUBTRACTION
LOSS
SHIFT
CONVERSION AND SUBTRACTION
CAPACITANCE, RANGE
STOP
STA
REI
800 μs
ARC3
R3
(RE2)
RI2
(L)
LPGP
ARCI2
A
STB
B
C
D
E
F
STBD
RE3
G
H
I
J
K
1781-15X

BLOCK

AQ

RI2 S021-1
12
L
LL S021-14
LLI S021-15
LL2 S021-16
LI S03
L2 S03
L3 S03
L4 S03
S025-12 LL
LI S02
L2 S025
S023-12 LL
L3 S02
L4 S023
LLI
LL2
LIMIT
RANGE


RING-OF-TWELVE BOARD, I
ARC12 S021-18
K J I H G F E D C B A
KK S021-11 JJ S021-8 II S021-5 HH S021-2 GG S020-23 FF S020-19 EE S020-15 DD S020-11 CC S020-8 BB S020-5 AA S020-1
KKI S021-12 JJI S021-9 III S021-6 HHI S021-3 GGI S020-24 EEI S020-16 DDI S020-12 CCI S020-9 BBI S020-6 AAI S020-2
KK2 S021-13 JJ2 S021-10 II2 S021-7 HH2 S021-4 GG2 S021-1 FF3 S020-22
BCD DATA INPUT SOCKET, AX
KI S030-BI JI S030-A2 II S030-B3 HI S030-A4 GI S030-B5 EI S030-A6 DI S030-B7 CI S030-A8 BI S030-B9 AI S030-A10
K2 S030-DI J2 S030-C2 I2 S030-D3 H2 S030-C4 G2 S030-D5 E2 S030-C6 D2 S030-D7 C2 S030-C8 B2 S030-D9 A2 S030-C10
K3 S030-FI J3 S030-E2 I3 S030-F3 H3 S030-E4 G3 S030-F5 E3 S030-E6 D3 S030-F7 C3 S030-E8 B3 S030-F9 A3 S030-E10
K4 S030-HI J4 S030-G2 I4 S030-H3 H4 S030-G4 G4 S030-H5 E4 S030-G6 D4 S030-H7 C4 S030-G8 B4 S030-H9 A4 S030-G10
REAR PARALLEL-SERIAL BOARD, J
KK S025-6 JJ S025-3 II S024-24 HH S024-21 GG S024-18 FF S024-15 EE S024-12 DD S024-9 CC S024-6 BB S024 3 AA
KI S025-7 JI S025-4 II S025-1 HI S024-22 GI S024-9 -15V EI S024-13 DI S024-10 CI S024-7 BI S024-4 AI S024-1 RE2 S025-17
K2 S025-8 J2 S025-5 I2 S025-2 H2 S024-23 G2 S024-20 E2 S024-14 D2 S024-11 C2 S024-8 B2 S024-5 A2 S024-2
SD Q CD Q
XI S025-18
ZXIC S025-20
1-BIT MEMORY FF
ZX2 S025-13
X2C S025-16
2-BIT MEMORY FF
FRONT PARALLEL-SERIAL BOARD, J
KK S023-6 JJ S023-3 II S022-24 HH S022-21 GG S022-18 FF S022-15 EE S022-12 DD S022-9 CC S022-6 BB S022-3 AA
K3 S023-7 J3 S023-4 I3 S023-1 H3 S022-22 G3 S022-19 -15V E3 S022-13 D3 S022-10 C3 S022-7 B3 S022-4 A3 S022-1 RE2 S023-17
K4 S023-8 J4 S023-5 I4 S023-2 H4 S022-23 G4 S022-20 E4 S022-14 D4 S022-11 C4 S022-8 B4 S022-5 A4 S022-2
SD Q CD Q
X4 S023-18
S023-20
ZX4C
4-BIT MEMORY FF
ZX8 S023-13
X8C S023-16
2' OR 8-BIT MEMORY FF
FORMAT BOARD, H
KKI JJI III HHI GGI
CAPACITANCE UPPER LIMIT
EEI DDI CCI BBI AAI
DISSIPATION/CONDUCTANCE UPPER LIMIT
UPPER CONVERTER
UIC S012-14
U2 S012-9
U4C S012-13
U8 S012-4
OUL THRU 9UL
KK2 JJ2 II2 HH2 GG2
CAPACITANCE LOWER LIMIT
LOWER CONVERTER
ZLI S012-22
ZL2C S012-18
ZL4 S013-4
ZL8C S012-16
OLL THRU 9LL


RING-OF-THREE
PART OF FORMAT BOARD, H
R3 S013-14
RE2
STB
ARC12
ARC3 S013-8
RE2 S013-13
STBD S013-6
STB S013-12
PROGRAM BOARD, G
R3 S019-10
R12 S019-3
600μS
RESET FF
ARC3 S019-19
20kHz CLOCK GEN
800 μS
PRINT COMMAND FF
PRT S031-C4
PRT S018-24
PRINT ALL
PRINT IN-TOL
PRINTOUT-OF-TOL
CKKo
CKo
DATA READY COMMAND CONTROL
START SCHMITT
STA S018-1
STAB S018-14
COMPARE
REI S018-22
RE2 S019-2
LPGP S018-3
STA S031-A4
STAB S031-E4
SUBTRACTOR BOARD, K
RELAY DRIVER BOARD, L
RELAY BOARD, L
LPGP S016-20
FF3 S014-15
RE2 S014-13
REI S014-14
STB S014-10
STBD S014-22
UPPER SUBTRACTOR
U1C
X1
B0
X2C
U2
U4C
X4
X8C
U8
HIGH C BORROW MEMORY
CD
SD
B0 S014-3
HIGH D/G BORROW MEMORY
REI
B0S S014-21
STBD
B0 S016-12
HICR S016, 11
HICL S016, 10
HIGH C
HC S027-8
HICNC S027-5
HICNO S027-6
HICR S027-7
HC S031-D5
HICNC S031-G2
HICNO S031-E2
B0S S016-6
HIDR S016-5
HIDL S016-4
HIGH D/G
HDC S027-18
HIDNC S027-11
HIDNO S027-14
HIDR S027-17
HDC S031, H5
HIDNC S031-H1
HIDNO S031-F1
FF3 S015-15
RE2 S015-13
REI S015-14
STB S015-10
STBD S015-19
LOWER SUBTRACTOR
ZX1C
ZL1
ZB0
ZL2C
ZX2
ZL4
ZX4C
ZL8C
ZX8
LOW C BORROW MEMORY
ZB0 S015-3
LOW D/G BORROW MEMORY
ZB0 S016-9
LOCR S016-8
LOCL S016-7
LOW C
GOR S016-17
GOL S016-16
GO
GOR S027-2
GC S027-3
GONC S027-1
GONO S027-4
GC S031-B5
GONC S031-D3
GONO S031-B3
LOCR S027-12
LC S027-13
LOCNC S027-9
LOCNO S027-10
LC S031-F5
LOCNC S031-C2
LOCNO S031-A2
JORITY AND-GATE (ONLY TWO OUT OF THREE INPUTS
ED BE PRESENT FOR AN OUTPUT)

FUNCTION	COLOR	CONNECTIONS
A	WH-OR-VT-BR	C518,A; S011,7; T51,16
AA	——	S020,1; S022,3; S024,3
AA1	WH-YE-BK	S020,2; S902,5-C
ARC3	WH-VT-BR-BK	S013,8; S019,19
ARC12	WH-GY-BL-BR	S013,17; S021,18
A1	WH-OR-GY-BK	S024,1; S030,A10; S032,A10
A2	WH-OR-GY-BR	S024,2; S030,C10; S032,C10
A3	WH-OR-GY-BL	S022,1; S030,E10; S032,E10
A4	WH-OR-GY-GN	S022,2; S030,G10; S032,G10
B	WH-YE-VT-RD	Q51,B; S011,8
BB	——	S020,5; S022,6; S024,6
BO	WH-VT-GN-BK	S014,3; S017,12
BOB	WH-YE-OR-BK	S014,11; S031,B9
BOS	WH-YE-OR-BL	S014,21; S017,6
BOSB	WH-OR-VT-BL	S014,20; S031,D9
BB1	WH-OR-BR	S020,6; S902,4-C
B1	WH-VT-GY-BK	S024,4; S030,B9; S032,B9
B2	WH-VT-GY-BR	S024,5; S030,D9; S032,D9
B3	WH-VT-GY-BL	S022,4; S030,F9; S032,F9
B4	WH-VT-GY-GN	S022,5; S030,H9; S032,H9
CC	——	S020,8; S022,9; S024,7
CK	WH-YE-GY-BL	S017,14; S032,E12; S903,106R
CK/CKK	WH-BL-BR-BK	S018,23; S903,108R
CKK	WH-GN-BR-BK	S017,15; S903,105R
CC1	WH-OR-BK	S020,9; S902,3-C
C1	WH-VT-RD-BK	S024,7; S030,A8; S032,A8
C2	WH-VT-RD-BR	S024,8; S030,C8; S032,C8
C3	WH-VT-RD-BL	S022,7; S030,E8; S032,E8
C4	WH-VT-RD-GN	S022,8; S030,G8; S032,G8
D	WH-OR-VT-BL	C52A,A; Q51,C; S011,9; T51,14
DD	——	S020,11; S022,12; S024,12
DD1	WH-VT-BR	S020,12; S902,2-C
D1	WH-GY-RD-BK	S024,10; S030,B7; S032,B7
D2	WH-GY-RD-BR	S024,11; S030,D7; S032,D7
D3	WH-GY-RD-BL	S022,10; S030,F7; S032,F7
D4	WH-GY-RD-GN	S022,11; S030,H7; S032,H7
EE	——	S020,15; S022,15; S024,15
EE1	WH-VT-BK	S020,16; S902,1-C
E1	WH-YE-BK	S024,13; S030,A6; S032,A6
E2	WH-YE-BR	S024,14; S030,C6; S032,C6
E3	WH-YE-BL	S022,13; S030,E6; S032,E6
E4	WH-YE-GN	S022,14; S030,G6; S032,G6
FF	——	S020,19; S022,18; S024,18
FF1	WH	S020,20; S902,5-D
FF3	WH-GY-GN-BK	S013,7; S014,15; S015,15; S020,22
F1	BL	S024,16 } COMMON CONNECTION (-15V)
F2	BL	S024,17 } COMMON CONNECTION (-15V)
F3	BL	S022,16 } COMMON CONNECTION (-15V)
F4	BL	S022,17 } COMMON CONNECTION (-15V)
G	WH-OR-RD-BL	Q52,B; S011,2
GC	WH-YE-BL-BR	S027,3; S031,B5
GG	——	S020,23; S022,21; S024,21
VREF	OR	C51,CASE; P901,R; P904,R; Q51,E; S011,6; S013,21; S015,21; S017,21; S019,21; S021,21; S023,21; S025,21; S027,21; S030,C12; S031,C12; S032,C12; S904,R; T51,6,C901,A; S903,104R
C GND	WH-YE-VT-GN	S011,3; S030,H13; S031,H13; S032,H13

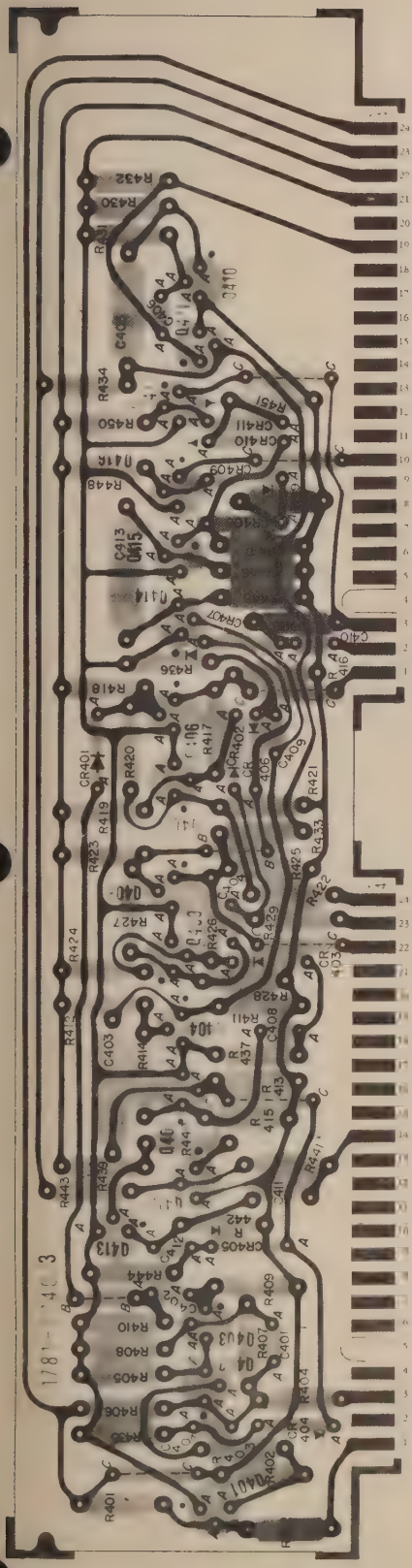
FUNCTION	COLOR	CONNECTIONS
GOL	WH-YE-OR	P906,L; S017,16
GONC	WH-OR-GN-BK	S027,1; S031,D3
GONO	WH-OR-GN-BR	S027,4; S031,B3
GOR	WH-RD-BL-BR	S017,17; S027,2
GG1	WH-GY-BR	S020,24; S901,11-C
GG2	WH-OR-RD-BK	S021,1; S901,6-C
G1	WH-OR-BK	S024,19; S030,B5; S032,B5
G2	WH-OR-BR	S024,20; S030,D5; S032,D5
G3	WH-OR-BL	S022,19; S030,F5; S032,F5
G4	WH-OR-GN	S022,20; S030,H5; S032,H5
HC	WH-OR-GN-BL	S027,8; S031,D5
HDC	WH-OR-RD-GN	S027,18; S031,H5
HH	——	S021,2; S022,24; S024,24
HICL	WH-BR-BK	P903,L; S017,10
HICNC	WH-OR-RD-BL	S027,5; S031,G2
HICNO	WH-YE-BR-BK	S027,6; S031,E2
HICR	WH-RD-BL-BK	S017,11; S027,7
HIDL	WH-GN-BR	P904,L; S017,4
HIDNC	WH-YE-GN-BR	S027,11; S031,H1
HIDNO	WH-OR-RD-BR	S027,14; S031,F1
HIDR	WH-GN-BL-BR	S017,5; S027,17
HH1	WH-RD-BR	S021,3; S901,10-C
HH2	WH-OR-GN-BL	S021,4; S901,5-C
H1	WH-VT-BK	S024,22; S030,A4; S032,A4
H2	WH-VT-BR	S024,23; S030,C4; S032,C4
H3	WH-VT-BL	S022,22; S030,E4; S032,E4
H4	WH-VT-GN	S022,23; S030,G4; S032,G4
II	——	S021,5; S023,3; S025,3
INH	WH-YE-GY-GN	S018,G; S030,G12; S032,G12
II1	WH-RD-BK	S021,6; S901,9-C
II2	WH-OR-GN-BR	S021,7; S901,4-C
I1	WH-GY-BK	S025,1; S030,B3; S032,B3
I2	WH-GY-BR	S025,2; S030,D3; S032,D3
I3	WH-GY-BL	S023,1; S030,F3; S032,F3
I4	WH-GY-GN	S023,2; S030,H3; S032,H3
JJ	——	S021,8; S023,6; S025,6
JJ1	WH-GY-BK	S021,9; S901,8-C
JJ2	WH-OR-GN-BK	S021,10; S901,3-C
J1	WH-RD-BK	S025,4; S030,A2; S032,A2
J2	WH-RD-BR	S025,5; S030,C2; S032,C2
J3	WH-RD-BL	S023,4; S030,E2; S032,E2
J4	WH-RD-GN	S023,5; S030,G2, S032,G2
KK	——	S021,11; S023,9; S025,9
KK1	WH-YE	S021,12; S901,7-C
KK2	WH-GN-BL	S021,13; S901,2-C
K1	WH-BK	S025,7; S030,B1; S032,B1
K2	WH-BR	S025,8; S030,D1; S032,D1
K3	WH-BL	S023,7; S030,F1; S032,F1
K4	WH-GN	S023,8; S030,H1; S032,H1
LC	WH-YE-OR-VT	S027,13; S031,F5
LDC	WH-YE-VT-GY	S027,19; S031,A6
LL	——	S021,14; S023,12; S025,12
LOCL	WH-VT-GY	S017,7; P902L

TION	COLOR	CONNECTIONS
NC	WH-YE-BL-BK	S027,9; S031,C2
NO	WH-OR-RD-BK	S027,10; S031,A2
CR	WH-RD-BR-BK	S017,8; S027,12
DL	WH-OR-VT	P904,R; S017,1
NC	WH-YE-GN-BK	S027,15; S031,D1
NO	WH-OR-VT-BK	S027,16; S031,B1
R	WH-GN-BL-BK	S017,2; S027,20
P	WH-OR	S017,20; S018,3
1	WH-YE-VT	S021,15; S901,1F-C
2	WH-GY-RD	S021,16; S901,1R-C
	WH-YE-RD-BK	S025,10; S030,B11; S032,B11
	WH-YE-RD-BR	S025,11; S030,D11; S032,D11
	WH-YE-RD-BL	S023,10; S030,F11; S032,F11
	WH-YE-RD-GN	S023,11; S030,H11; S032,H11
T	WH-YE-GY-BK	S018,24; S032,A12; S031,C4
1	WH-OR-GY-RD	S014,14; S015,14; S018,22
2	WH-VT-GN-BR	S013,13; S014,13; S015,13; S019,2; S023,17; S025,17
	WH-GY-GN-BR	S013,14; S019,10
2	WH-YE-OR-GY	S019,3; S021,17
A	WH-YE-GY-BK	S018,1; S030,A12; S031,A4
AB	WH-BL-BK	S018,14; S904,L; S031,E4
B	WH-OR-BL-BK	S013,12; S014,10; S015,10
BD	WH-VT-BL-BK	S013,6; S014,22, S015,19
C	WH-YE-OR-BR	S012,14; S014,1
	WH-OR-VT-RD	S012,9; S014,4
C	WH-OR-VT-GN	S012,13; S014,6
	WH-YE-GN-BL	S012,4; S014,8
	WH-RD-GN-BR	S014,2; S025,18
C	WH-GY-BR-BK	S014,5; S025,16
	WH-RD-GN-BL	S014,7; S023,18
C	WH-OR-BR-BK	S014,9; S023,16
O	WH-YE-GY-RD	S015,3; S017,9
OB	WH-YE-VT-RD	S015,11; S031,F9
OS	WH-YE-OR-GN	S015,18; S017,3
OSB	WH-OR-VT-BR	S015,16; S031,H9
1	WH-OR-VT-GY	S012,22; S015,1
2C	WH-VT-BL-BR	S012,18; S015,4
4	WH-OR-BL-BR	S013,4; S015,6
8C	WH-GY-GN-BL	S012,16; S015,8
1C	WH-RD-GN-BK	S015,2; S025,20
2	WH-VT-GN-BL	S015,6; S025,13
4C	WH-GY-BL-BK	S015,7; S023,20
8	WH-VT-GY-RD	S015,9; S023,13
	WH-GY	S012,17; S901,6-1
	GN	S012,19; S901,6-2
	WH-YE-BL-BK	S012,20; S901,6-3
	WH-OR-RD-BR	S012,21; S901,6-4
L	WH-OR-VT-BK	S012,23; S901,6-5

FUNCTION	COLOR	CONNECTIONS
6LL	WH-YE-VT-GY	S018,24; S901,6-6
7LL	WH-YE-OR-VT	S013,1; S901,6-7
8LL	WH-VT	S013,2; S901,6-8
9LL	GY	S013,3; S901,6-9
1UL	WH-YE-GY	S012,11; S901,1F-1
2UL	WH-BL-BR	S012,10; S901,1F-2
3UL	WH-OR-GY	S012,8; S901,1F-3
4UL	WH-YE-RD	S012,7; S901,1F-4
6UL	WH-VT-RD	S012,5; S901,1F-6
7UL	WH-GN-BK	S012,3; S901,1F-7
8UL	WH-RD	S012,2; S901,1F-8
9UL	VT	S012,1; S901,1F-9
ØLL	WH-YE-BR-BK	S012,15; S901,6-0
ØUL	WH-OR-RD	S012,12; S901,1F-0
+6V	RD	S011,4; S013,22; S015,22; S017,22; S019,22; S023,22; S025,22; S027,22
-15V	BL	C52,CASE; Q52,E; S011,10; S013,24; S015,24; S017,24; S019,24; S021,24; S023,24; S025,24; TS4,15, S027,24 C901,CASE
-21V	BR	C53,CASE; S011,1; S013,23; S015,23; S017,23; S019,23; S021,23; S023,23; S025,23; TS4,11, S027,23

S011
-21V
G
C GND
+6V
VREF
A
B
D
-15V
S012
9UL
8UL
7UL
U8
6UL
4UL
3UL
U2
S014
J1C
X1
BO
U2
X2C
U4C
X4
U8
X8C
S018
STA
LPSP
INH
S020
AA
AAI
BB
BBI
CC
CCI
S022
A3
A4
AA
B3
B4
BB
C3
C4
CC
S024
A1
A2
AA
B1
B2
BB
C1
C2
CC
A
B
C
D
E
F
G
H
J1
K1
J2
K2
J3
K3
J4
K4

S013
S015
S017
S019
S021
S023
S025
S027
BCD DATA OUTPUT
RELAY CONTACTS OUTPUT
BCD DATA OUTPUT
S030
S031
S032

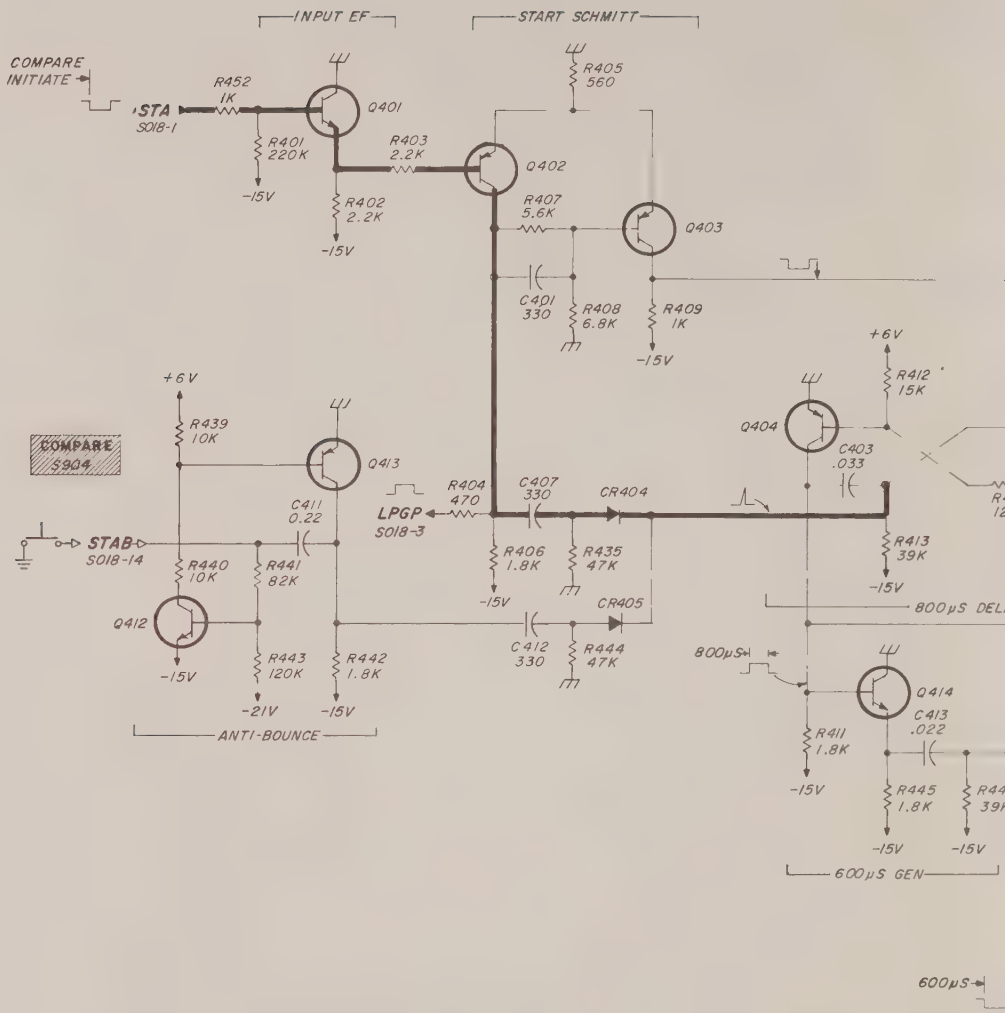


SO19 RIGHT

24	-15V	POWER
23	-21V	POWER
22	+6V	POWER
21	VREF (+)	POWER
20		
19	ARC 3	CLOCK PULSES
18		
17		
16		
15		
14		
13		
12		
11		
10	R3	SET
9		
8		
7		
6		
5		
4		
3	R12	SET
2	RE2	RESET
1	PRT	PRINT COMMAND COMPLEMENT

SO18 LEFT

24	PRT	PRINT COMMAND
23	CK-CKK	GO- NO GO
22	RE1	RESET
21		
20		
19		
18		
17		
16		
15		
14	STAB	COMPARE INITIATE
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3	LPGP	DRIVER ENABLE
2		
1	STA	COMPARE INITIATE



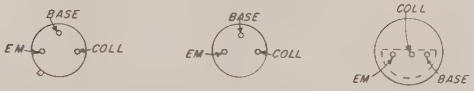
• SIGNAL DIRECTION

- OUTPUT TO ANOTHER DIAGRAM
- INPUT FROM ANOTHER DIAGRAM
- OUTPUT REMAINS ON DIAGRAM
- INPUT FROM SAME DIAGRAM

• FLOATING GROUND

VREF(⏚) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS(S030,31,32)

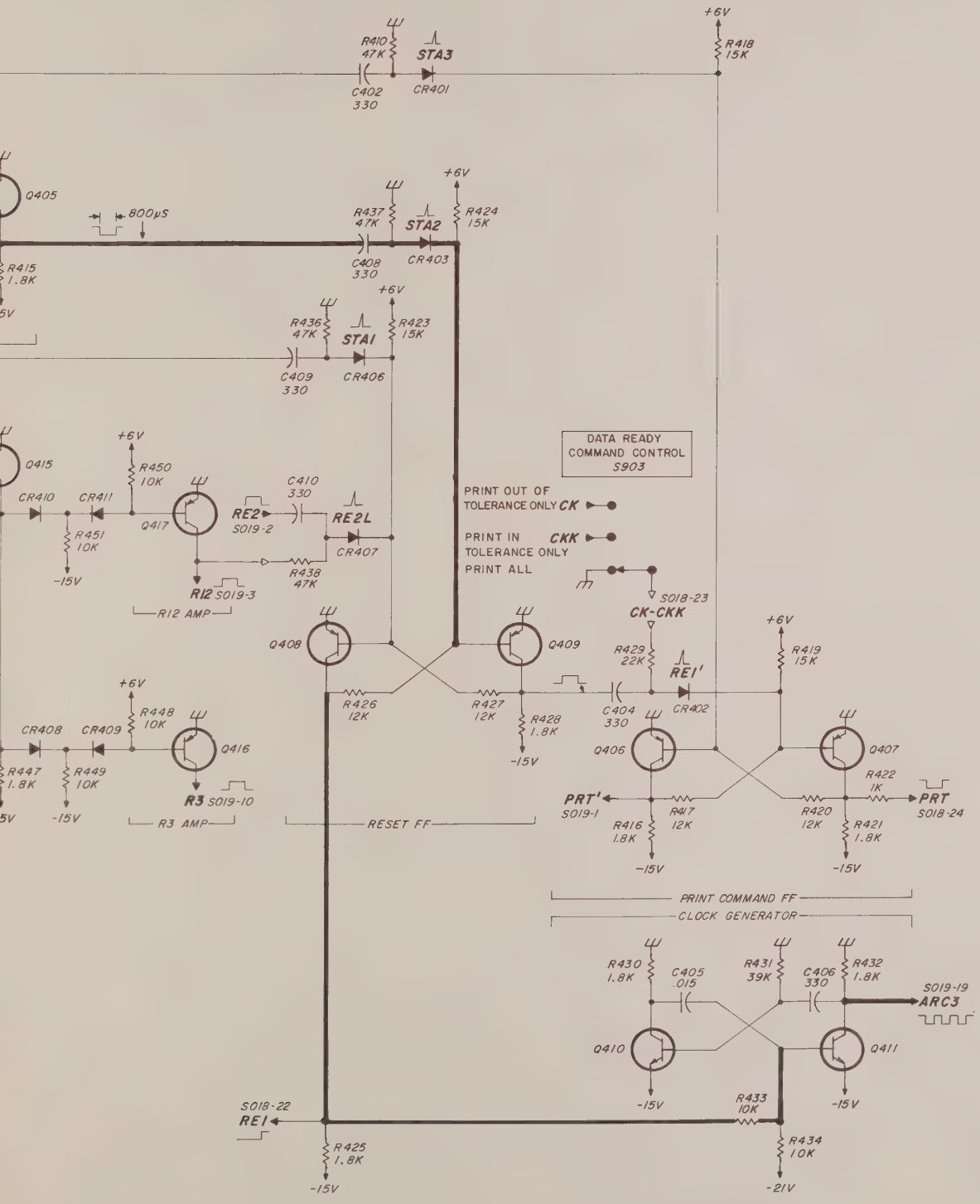
• TRANSISTORS

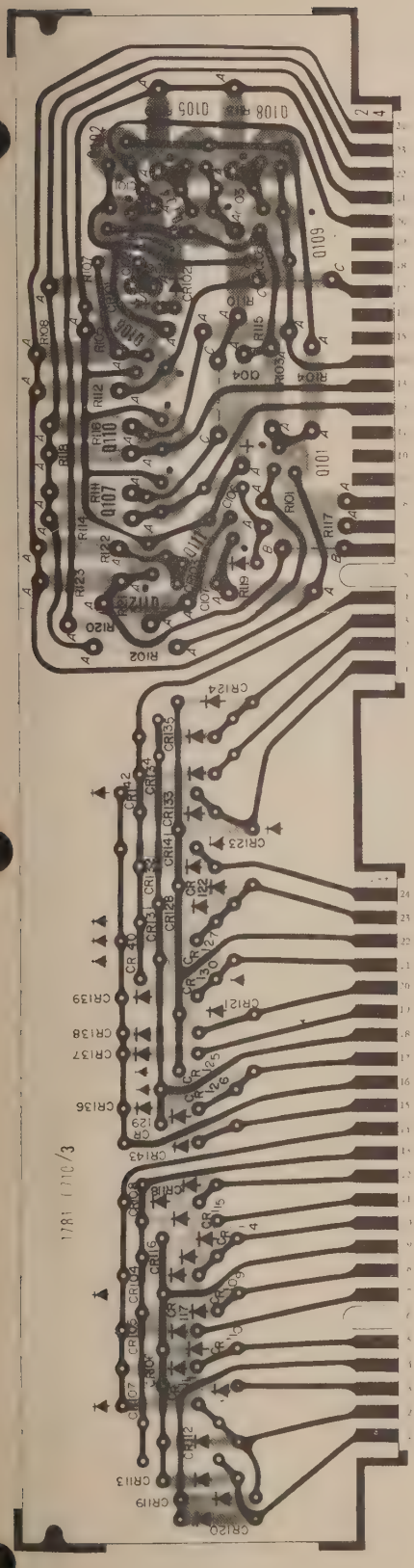


Q402 THRU Q411
Q413 THRU Q415

BOTTOM VIEW
Q416, Q417

Q401, Q412


R410 47K
STA3
C402 330
CR401
+6V
R418 15K
Q405
800μS
R437 47K
STA2
R424 15K
C408 330
CR403
R415 1.8K
R436 47K
STA1
R423 15K
C409 330
CR406
DATA READY COMMAND CONTROL S903
PRINT OUT OF TOLERANCE ONLY CK
PRINT IN TOLERANCE ONLY CKK
PRINT ALL
Q415
R450 10K
CR410
CR411
R451 10K
Q417
RE2 S019-2
C410 330
RE2L
CR407
R438 47K
RI2 S019-3
RI2 AMP
S018-23
CK-CKK
Q408
Q409
R429 22K
RE1'
R419 15K
R426 12K
R427 12K
R428 1.8K
C404 330
CR402
Q406
Q407
R422 1K
PRT'
S019-1
PRT
S018-24
R416 1.8K
R417 12K
R420 12K
R421 1.8K
R448 10K
CR408
CR409
Q416
R447 1.8K
R449 10K
R3 S019-10
R3 AMP
RESET FF
PRINT COMMAND FF
CLOCK GENERATOR
R430 1.8K
C405 .015
R431 39K
C406 330
R432 1.8K
S019-19
ARC3
Q410
Q411
R433 10K
S018-22
RE1
R425 1.8K
R434 10K
-15V
-21V

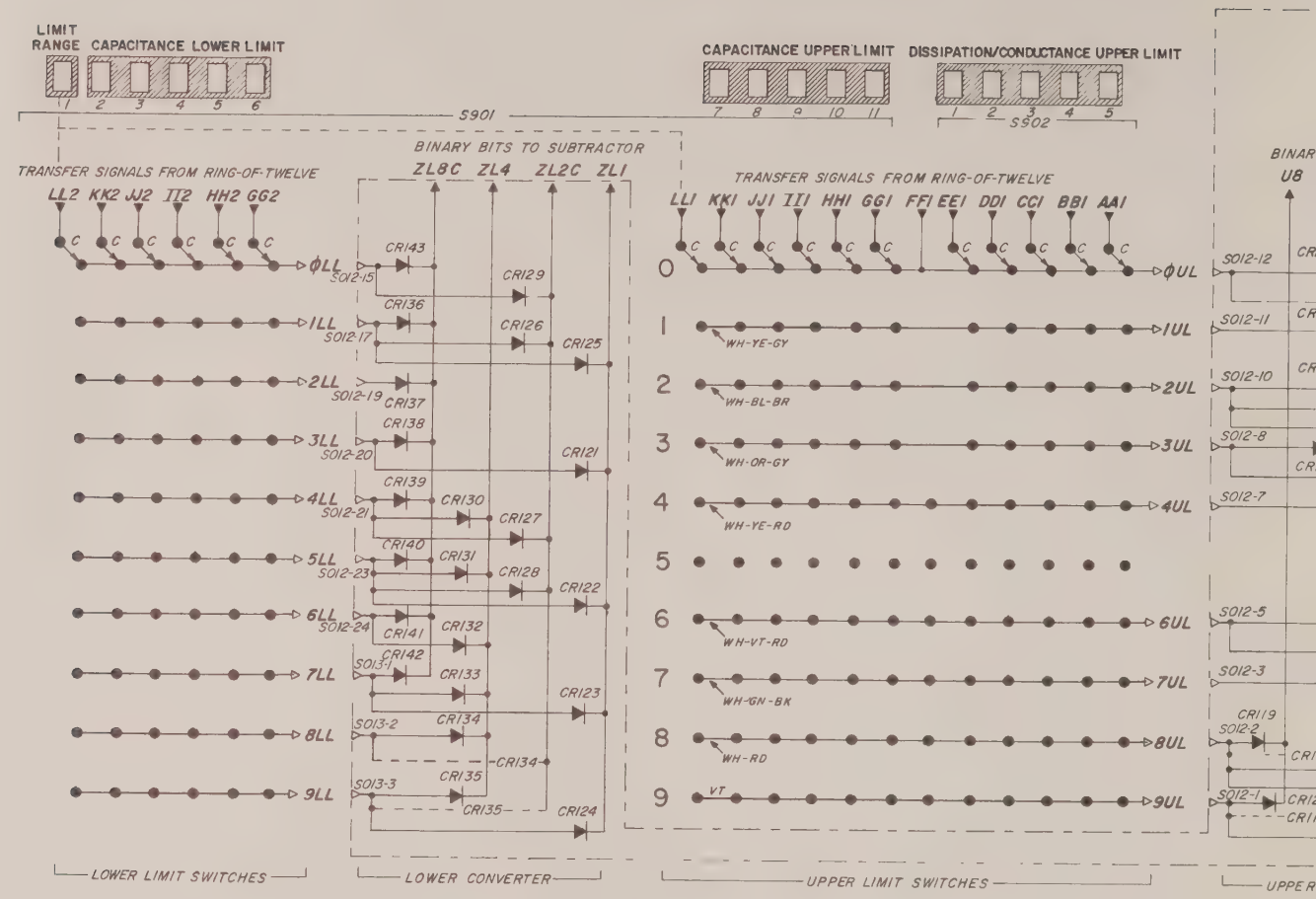


SO13 RIGHT

	-15V	POWER
	-21V	POWER
	+6V	POWER
	VREF (+)	FLOATING GROUND
	NOT USED	
	ARC 12	DRIVE
	R3	SET
	RE2	RESET
	STB	STORE BORROW
	ARC3	CLOCK PULSES
	FF3	SHIFT ENABLE
	STBD	STORE BORROW
	ZL4	LOWER LIMIT 4-BIT
	9LL	LOWER LIMIT DECIMAL 9
	8LL	LOWER LIMIT DECIMAL 8
	7LL	LOWER LIMIT DECIMAL 7

SO12 LEFT

24	6LL	LOWER LIMIT DECIMAL 6
23	5LL	LOWER LIMIT DECIMAL 5
22	ZL1	LOWER LIMIT 1-BIT
21	4LL	LOWER LIMIT DECIMAL 4
20	3LL	LOWER LIMIT DECIMAL 3
19	2LL	LOWER LIMIT DECIMAL 2
18	ZL2C	LOWER LIMIT 2-BIT COMPLEMENTED
17	1LL	LOWER LIMIT DECIMAL 1
16	ZL8C	LOWER LIMIT 2' OR 8-BIT COMPLEMENT
15	0LL	LOWER LIMIT DECIMAL 0
14	U1C	UPPER LIMIT 1-BIT COMPLEMENT
13	U4C	UPPER LIMIT 4-BIT COMPLEMENT
12	0UL	UPPER LIMIT DECIMAL 0
11	1UL	UPPER LIMIT DECIMAL 1
10	2UL	UPPER LIMIT DECIMAL 2
9	U2	UPPER LIMIT 2-BIT
8	3UL	UPPER LIMIT DECIMAL 3
7	4UL	UPPER LIMIT DECIMAL 4
6	6UL	UPPER LIMIT DECIMAL 6
5	U8	UPPER LIMIT 2' OR 8-BIT
4	7UL	UPPER LIMIT DECIMAL 7
3	8UL	UPPER LIMIT DECIMAL 8
2	9UL	UPPER LIMIT DECIMAL 9



• SIGNAL DIRECTION

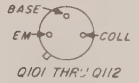
→ OUTPUT TO ANOTHER DIAGRAM
← INPUT FROM ANOTHER DIAGRAM
→ OUTPUT REMAINS ON DIAGRAM
← INPUT FROM SAME DIAGRAM

• FLOATING GROUND

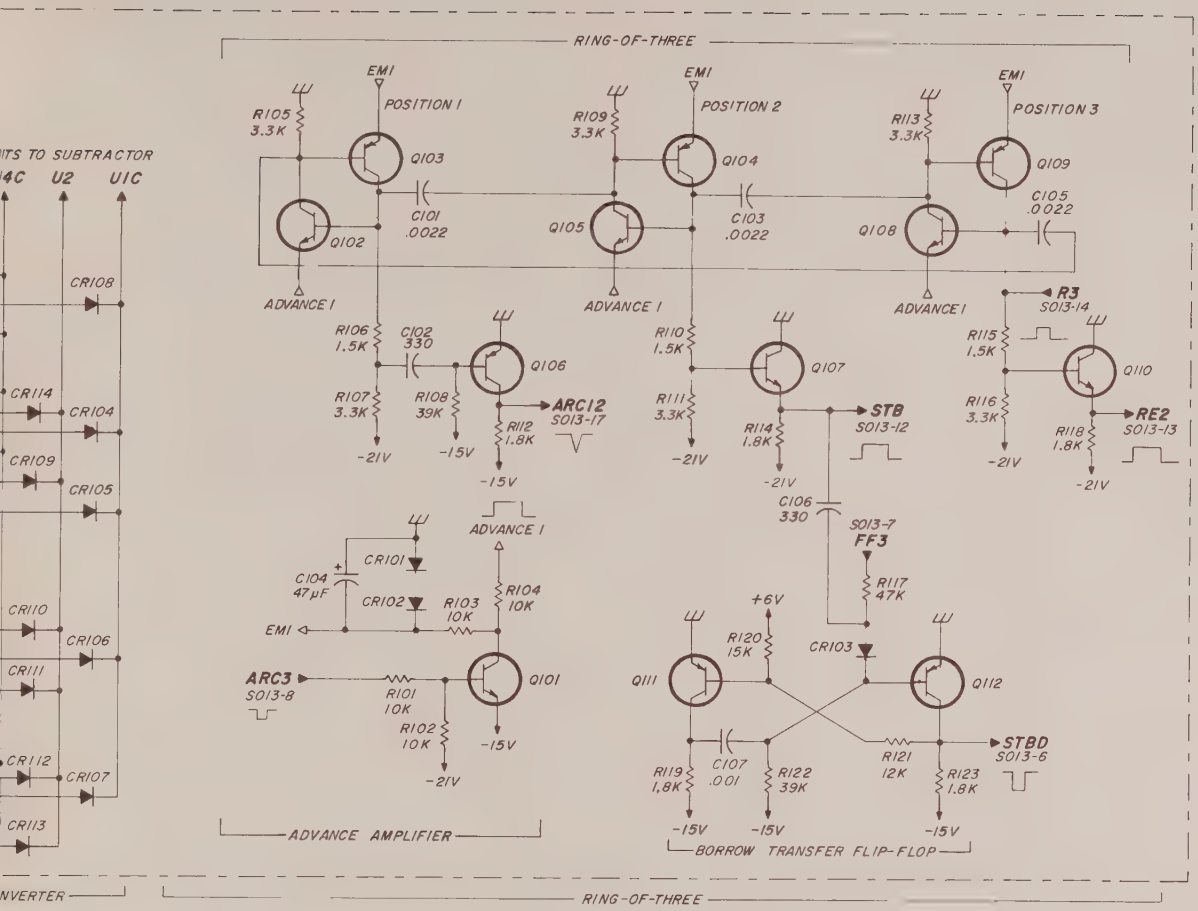
VREF(-77) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS (S030, 31, 32)

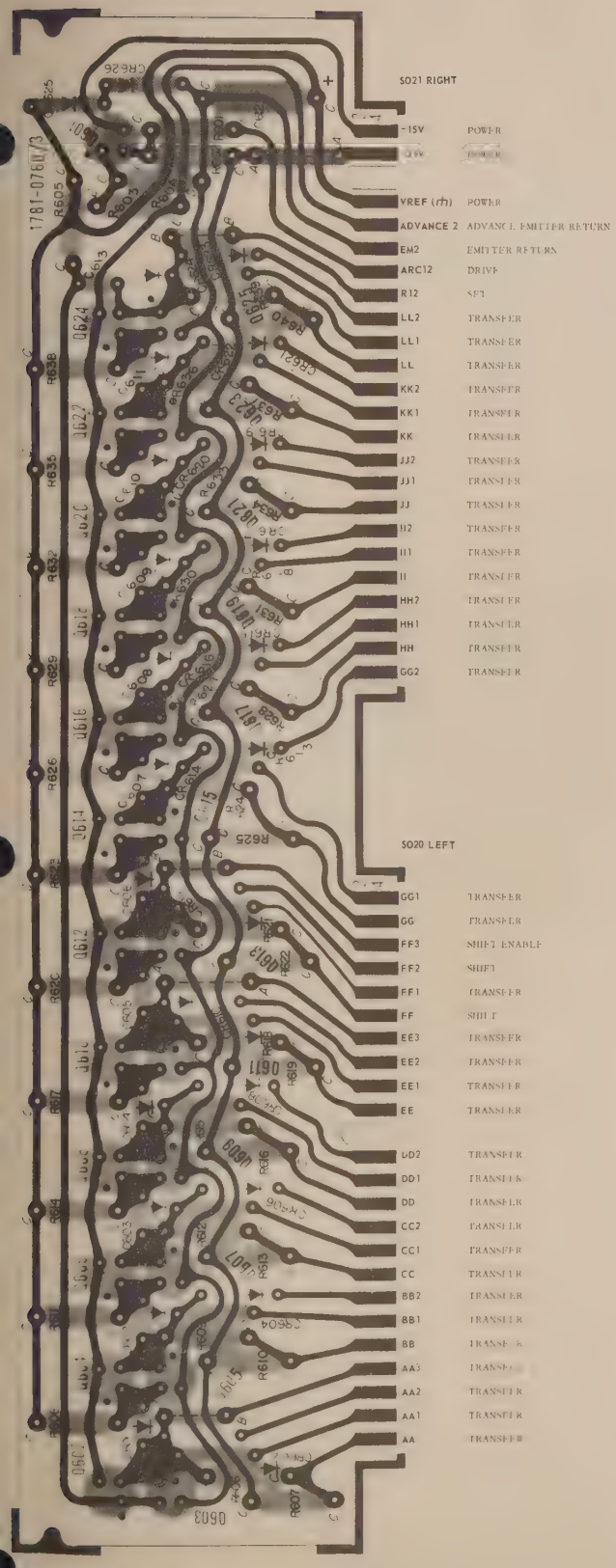
• TRANSISTORS

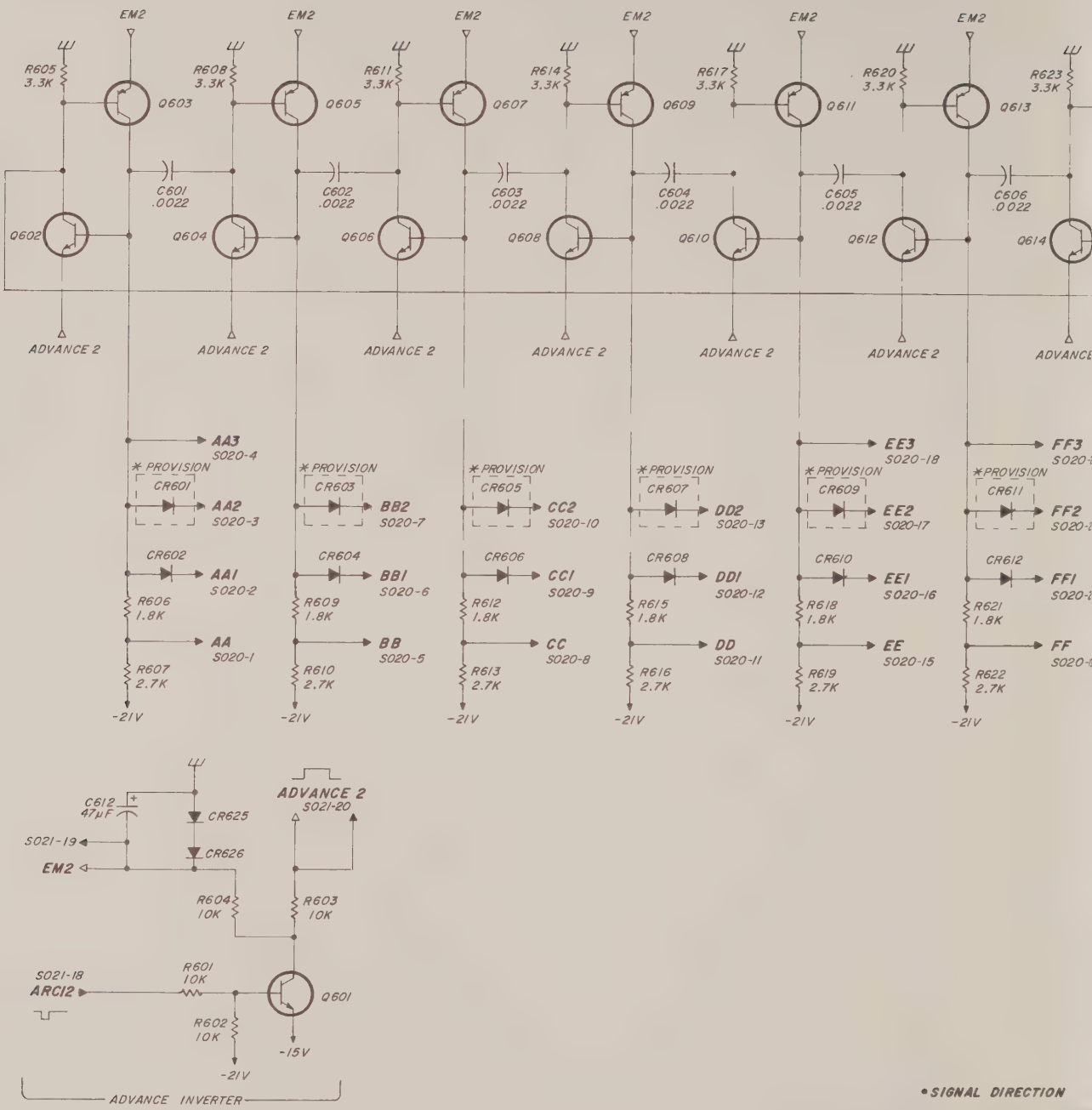
BOTTOM VIEW



Q101 THRU Q112


RING-OF-THREE
EMI
POSITION 1
POSITION 2
POSITION 3
R105 3.3K
R109 3.3K
R113 3.3K
Q103
Q104
Q109
Q102
Q105
Q108
C101 .0022
C103 .0022
C105 .0022
ADVANCE I
R106 1.5K
C102 330
R107 3.3K
R108 39K
R112 1.8K
Q106
-21V
-15V
ARC12 S013-17
R110 1.5K
R111 3.3K
R114 1.8K
Q107
STB S013-12
R3 S013-14
R115 1.5K
R116 3.3K
R118 1.8K
Q110
RE2 S013-13
C106 330
S013-7
FF3
R117 47K
+6V
R120 15K
CR103
Q111
Q112
R119 1.8K
C107 .001
R122 39K
R121 12K
R123 1.8K
STBD S013-6
BORROW TRANSFER FLIP-FLOP
C104 47μF
CR101
CR102
R103 10K
R104 10K
EMI
ARC3 S013-8
R101 10K
R102 10K
Q101
ADVANCE AMPLIFIER
ITS TO SUBTRACTOR
4C U2 U1C
CR108
CR114
CR104
CR109
CR105
CR110
CR106
CR111
CR112
CR107
CR113
NVERTER
RING-OF-THREE


SO21 RIGHT
-15V POWER
VREF (rh) POWER
ADVANCE 2 ADVANCE EMITTER RETURN
EM2 EMITTER RETURN
ARC12 DRIVE
R12 SET
LL2 TRANSFER
LL1 TRANSFER
LL TRANSFER
KK2 TRANSFER
KK1 TRANSFER
KK TRANSFER
JJ2 TRANSFER
JJ1 TRANSFER
JJ TRANSFER
II2 TRANSFER
II1 TRANSFER
II TRANSFER
HH2 TRANSFER
HH1 TRANSFER
HH TRANSFER
GG2 TRANSFER
SO20 LEFT
GG1 TRANSFER
GG TRANSFER
FF3 SHIFT ENABLE
FF2 SHIFT
FF1 TRANSFER
FF SHIFT
EE3 TRANSFER
EE2 TRANSFER
EE1 TRANSFER
EE TRANSFER
DD2 TRANSFER
DD1 TRANSFER
DD TRANSFER
CC2 TRANSFER
CC1 TRANSFER
CC TRANSFER
BB2 TRANSFER
BB1 TRANSFER
BB TRANSFER
AA3 TRANSFER
AA2 TRANSFER
AA1 TRANSFER
AA TRANSFER



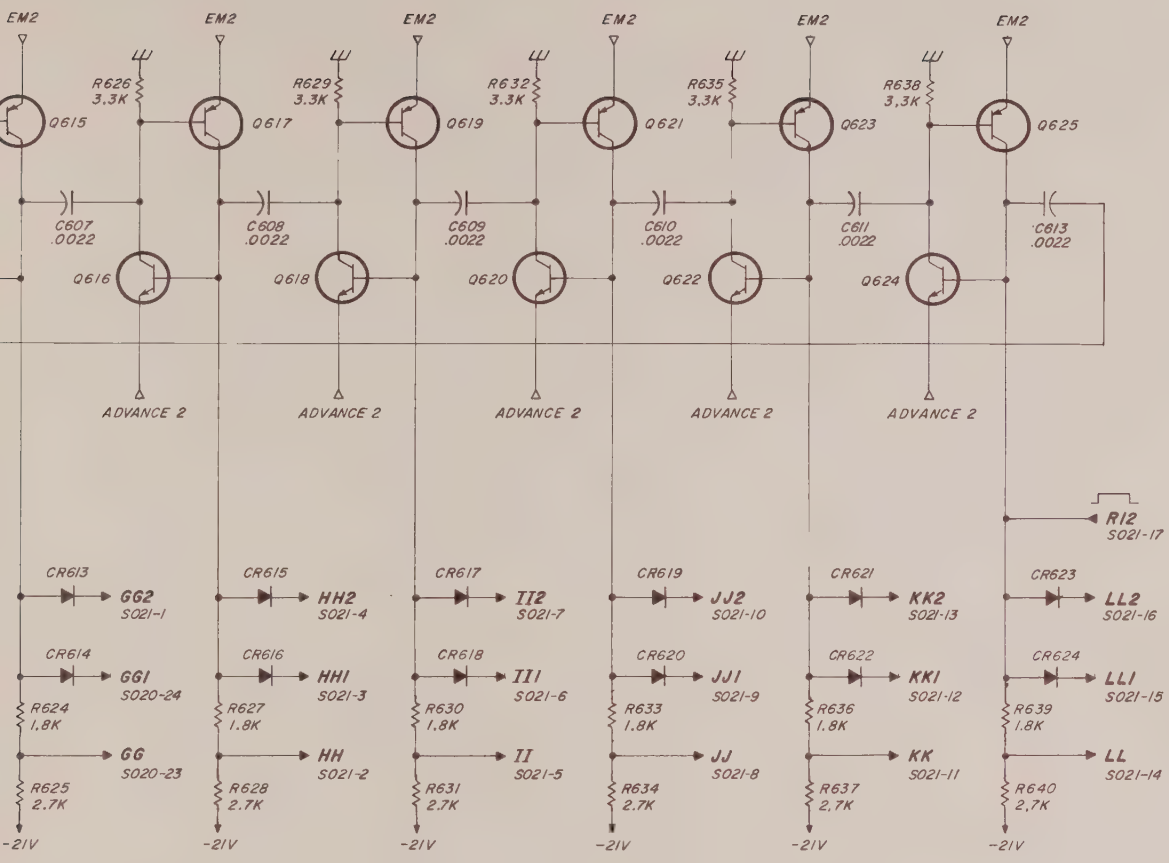
• SIGNAL DIRECTION

→ OUTPUT TO ANOTHER DIAGRA

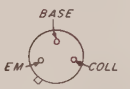
▶— INPUT FROM ANOTHER DIAGRA

—▷ OUTPUT REMAINS ON DIAGRA

—▷— INPUT FROM SAME DIAGRAM



• TRANSISTORS



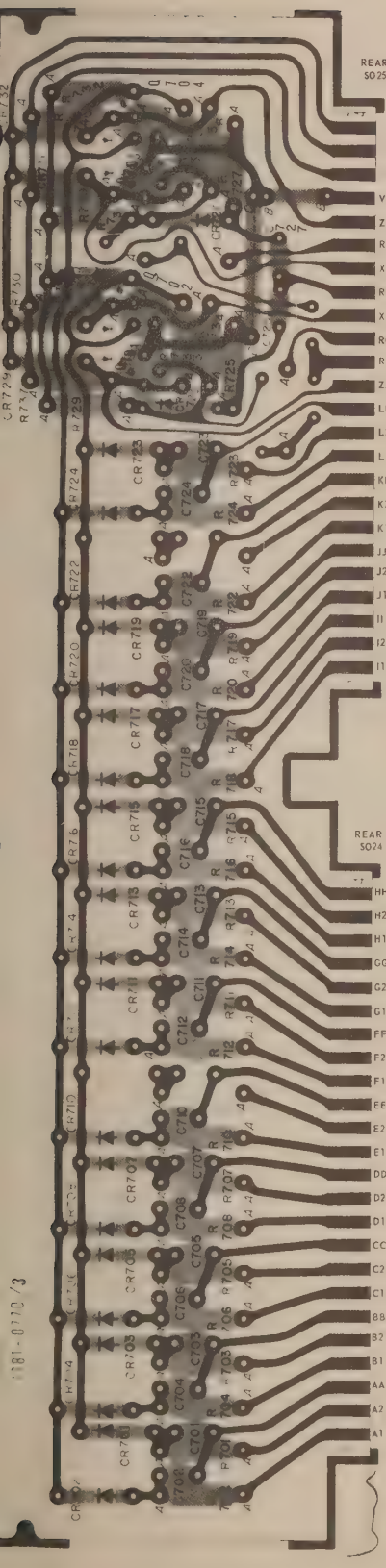
BOTTOM VIEW
Q601 THRU Q625

• FLOATING GROUND

VREF(-17) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS (SO30,31,32)

• LOW D

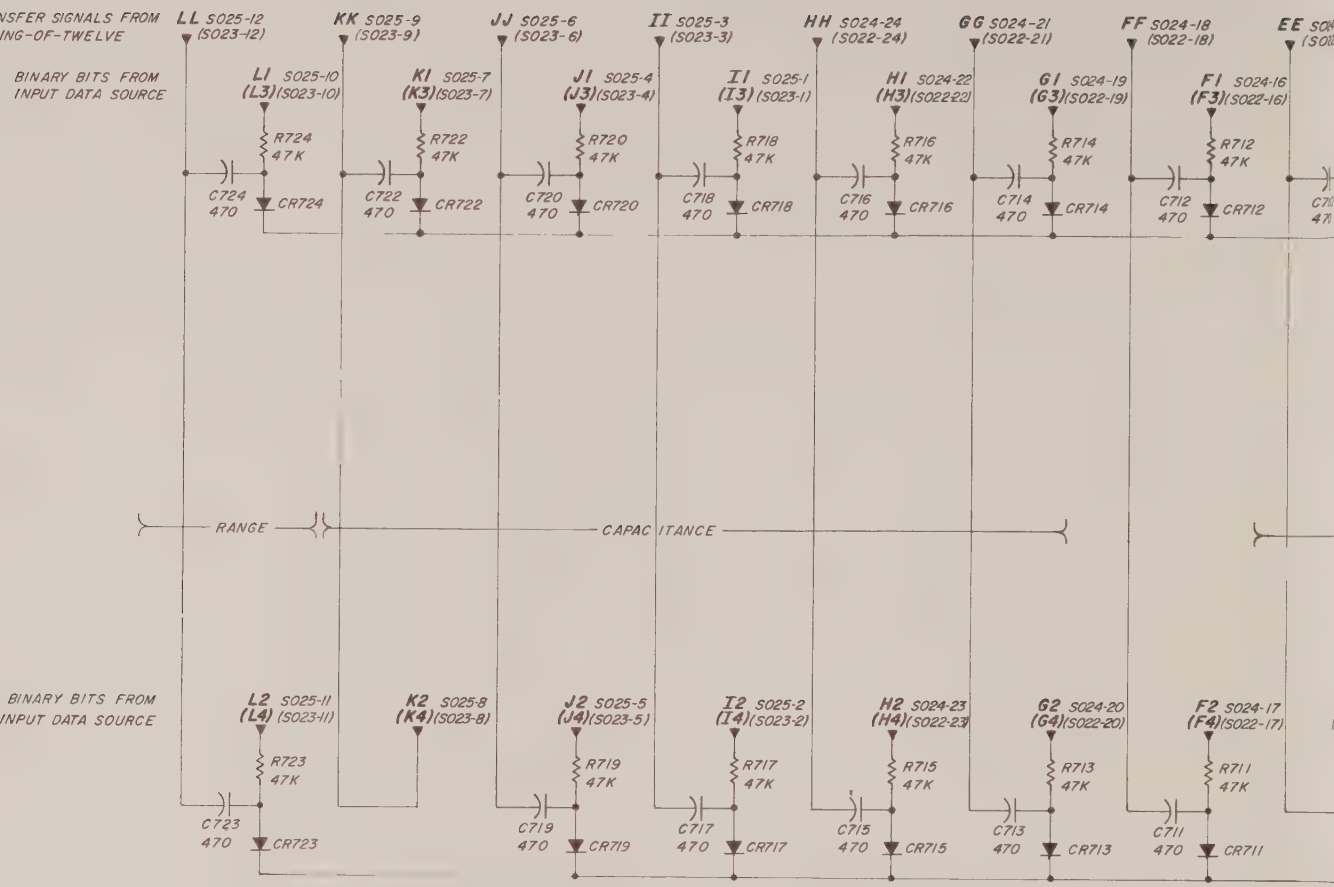
* PROVISION HAS BEEN MADE FOR LOW D COMPARISIONS; WIRING IS PRESENT BUT COMPONENTS ARE NOT



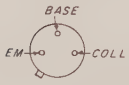
REAR BOARD SO25 RIGHT	FRONT BOARD SO23 RIGHT
15V	POWER
21V	POWER
6V	POWER
VREF (⏚)	FLOATING GROUND
ZX1C (ZX4C)	INPUT BIT
RG	NOT USED
X1, (X4)	INPUT BIT
RE2	RESET, D401
X2C, (X8C)	INPUT BIT
RG2	NOT USED
R	NOT USED
ZX2 (ZX8)	INPUT BIT
LL	TRANSFER
L2 (L4)	INPUT BIT
L1 (L3)	INPUT BIT
KK	TRANSFER
K2 (K4)	INPUT BIT
K1 (K3)	INPUT BIT
JJ	TRANSFER, D605
J2 (J4)	INPUT BIT
J1 (J3)	INPUT BIT
II	TRANSFER, D601
I2 (I4)	INPUT BIT
I1 (I3)	INPUT BIT

REAR BOARD SO24 LEFT	FRONT BOARD SO22 LEFT
HH	TRANSFER
H2 (H4)	INPUT BIT
H1 (H3)	INPUT BIT
GG	TRANSFER
G2 (G4)	INPUT BIT
G1 (G3)	INPUT BIT
FF	SHIFT
F2 (F4)	−15V
F1 (F3)	−15V
EE	TRANSFER
E2 (E4)	INPUT BIT
E1 (E3)	INPUT BIT
DD	TRANSFER
D2 (D4)	INPUT BIT
D1 (D3)	INPUT BIT
CC	TRANSFER
C2 (C4)	INPUT BIT
C1 (C3)	INPUT BIT
BB	TRANSFER
B2 (B4)	INPUT BIT
B1 (B3)	INPUT BIT
AA	TRANSFER
A2 (A4)	INPUT BIT
A1 (A3)	INPUT BIT

D NUMBERS INDICATE OTHER DIAGRAMS WHERE SIGNAL IS USED. ONLY MAJOR USES ARE SHOWN. FOR COMPLETE INTERCONNECTION INFORMATION, SEE D9001.



• TRANSISTORS



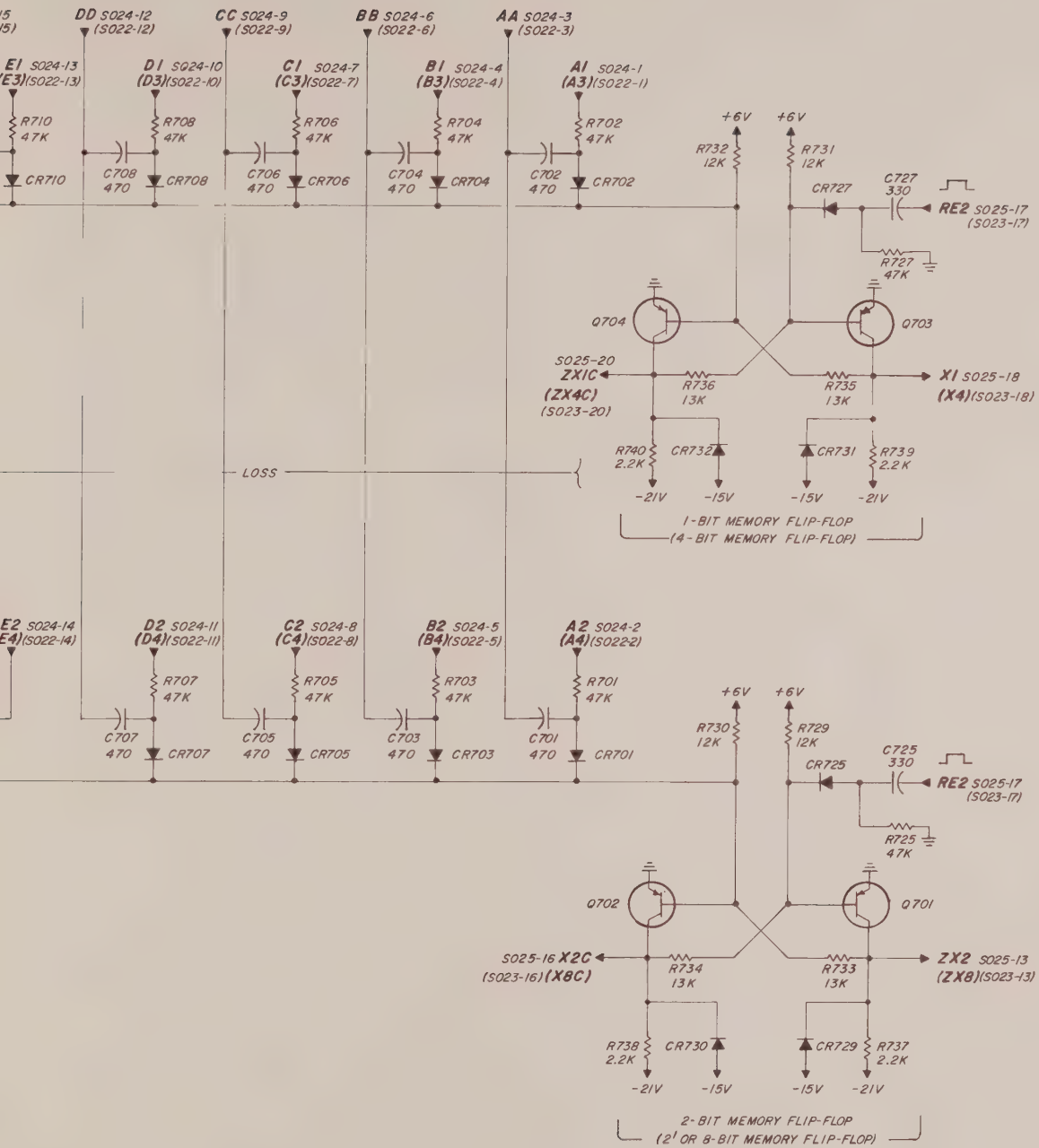
BOTTOM VIEW
Q701-Q704

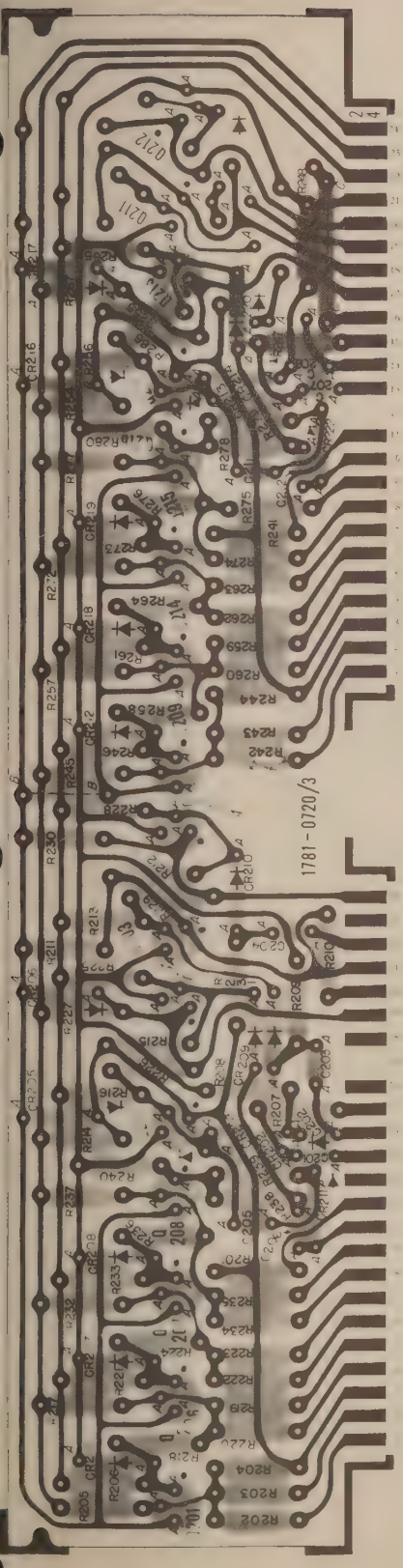
• SIGNAL DIRECTION

- OUTPUT TO ANOTHER DIAGRAM
- INPUT FROM ANOTHER DIAGRAM
- OUTPUT REMAINS ON DIAGRAM
- INPUT FROM SAME DIAGRAM

• FLOATING GROUND

VREF (+) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS (S030,31,32)


DD S024-12 (S022-12)
CC S024-9 (S022-9)
BB S024-6 (S022-6)
AA S024-3 (S022-3)
D1 S024-10 (D3)(S022-10)
C1 S024-7 (C3)(S022-7)
B1 S024-4 (B3)(S022-4)
A1 S024-1 (A3)(S022-1)
R710 47K
R708 47K
R706 47K
R704 47K
R702 47K
CR710
C708 470
CR708
C706 470
CR706
C704 470
CR704
C702 470
CR702
+6V
+6V
R732 12K
R731 12K
CR727
C727 330
RE2 S025-17 (S023-17)
R727 47K
Q704
Q703
S025-20 ZX1C (ZX4C) (S023-20)
R736 13K
R735 13K
X1 S025-18 (X4)(S023-18)
R740 2.2K
CR732
CR731
R739 2.2K
LOSS
-21V
-15V
-15V
-21V
1-BIT MEMORY FLIP-FLOP
(4-BIT MEMORY FLIP-FLOP)
D2 S024-11 (D4)(S022-11)
C2 S024-8 (C4)(S022-8)
B2 S024-5 (B4)(S022-5)
A2 S024-2 (A4)(S022-2)
R707 47K
R705 47K
R703 47K
R701 47K
C707 470
CR707
C705 470
CR705
C703 470
CR703
C701 470
CR701
+6V
+6V
R730 12K
R729 12K
CR725
C725 330
RE2 S025-17 (S023-17)
R725 47K
Q702
Q701
S025-16 X2C (S023-16)(X8C)
R734 13K
R733 13K
ZX2 S025-13 (ZX8)(S023-13)
R738 2.2K
CR730
CR729
R737 2.2K
-21V
-15V
-15V
-21V
2-BIT MEMORY FLIP-FLOP
(2' OR 8-BIT MEMORY FLIP-FLOP)



SO15 RIGHT

14	-15V	POWER
15	-21V	POWER
3	+6V	POWER
21	VREF (/7)	FLOATING GROUND
4	ZBOSC	LOW D BORROW COMPLEMENT
17	STBD	STORE BORROW
18	ZBOS	LOW D BORROW
19	ZBOC	LOW C BORROW COMPLEMENT
16	ZBOSB	LOW D BORROW
12	FF3	SHIFT ENABLE
23	RE1	RESET
13	RE2	RESET
11	ZBOB	LOW C BORROW
2	STB	C STORE BORROW
5	ZX8	INPUT 2' OR 8-BIT
8	ZL8C	LIMIT 2' OR 8-BIT COMPLEMENT
7	ZX4C	INPUT 4-BIT COMPLIMENT
	ZL4	LIMIT 4-BIT
6	ZX2	INPUT 2-BIT
9	ZL2C	LIMIT 2-BIT COMPLEMENT
10	ZBO	LOW C BORROW
1	ZX1C	INPUT 1-BIT COMPLEMENT
24	ZL1	LIMIT 1-BIT

SO14 LEFT

	BOSC	HIGH D BORROW COMPLEMENT
	STBD	D STORE BORROW
1	BOS	HIGH D BORROW
	BOSB	HIGH D BORROW
	BOC	HIGH C BORROW COMPLEMENT
	FF3	SHIFT ENABLE
23	RE1	RESET
	RE2	RESET
	BOB	HIGH C BORROW
	STB	C STORE BORROW
	X8C	INPUT 2' OR 8-BIT COMPLIMENT
8	U8	LIMIT 2' OR 8-BIT
	X4	INPUT 4-BIT
	U4C	LIMIT 4-BIT COMPLIMENT
	X2C	INPUT 2-BIT COMPLIMENT
	U2	LIMIT 2-BIT
	BO	HIGH C BORROW
	X1	INPUT 1-BIT
	U8C	LIMIT 1-BIT COMPLEMENT

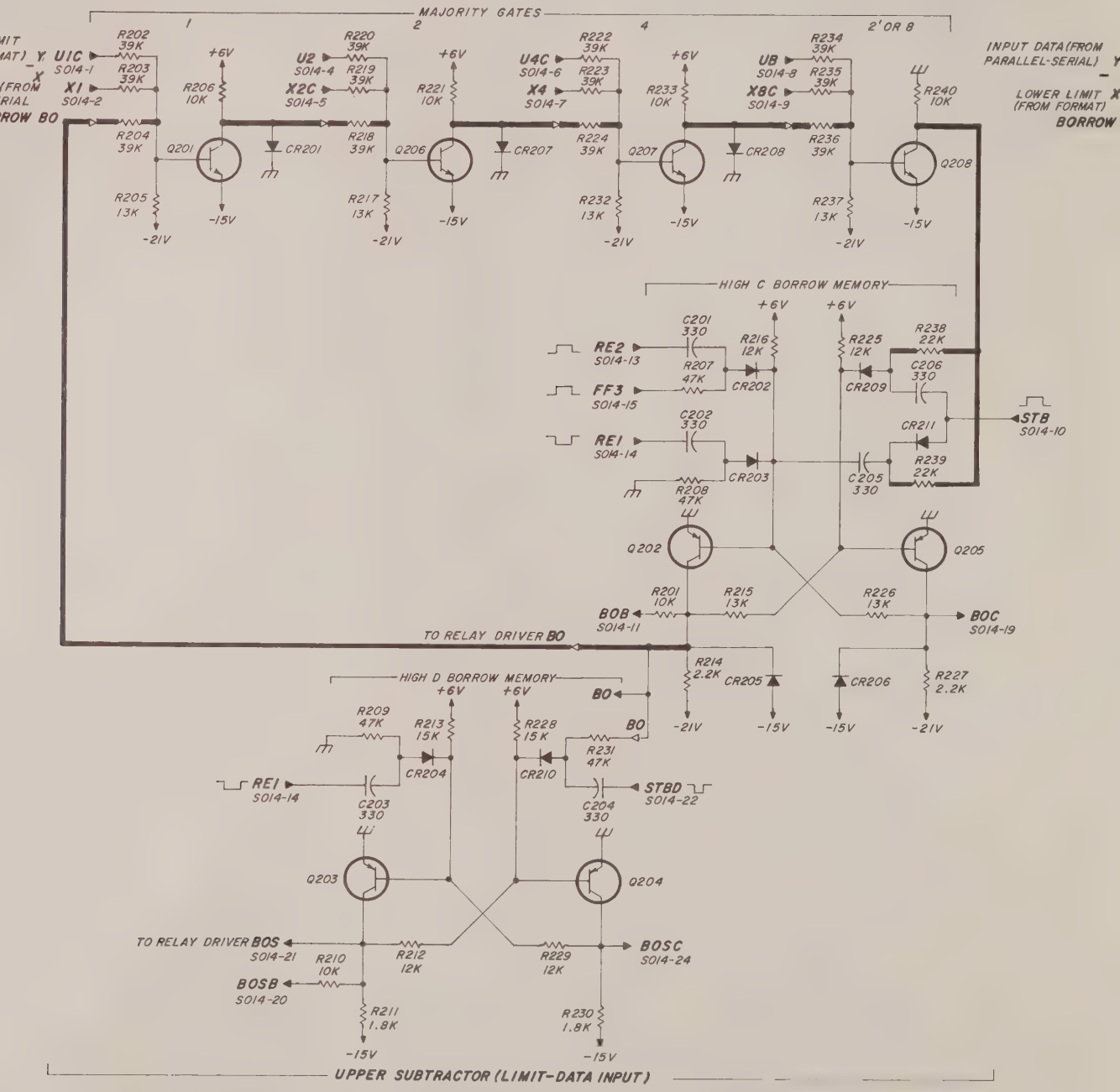
UPP
(FRC

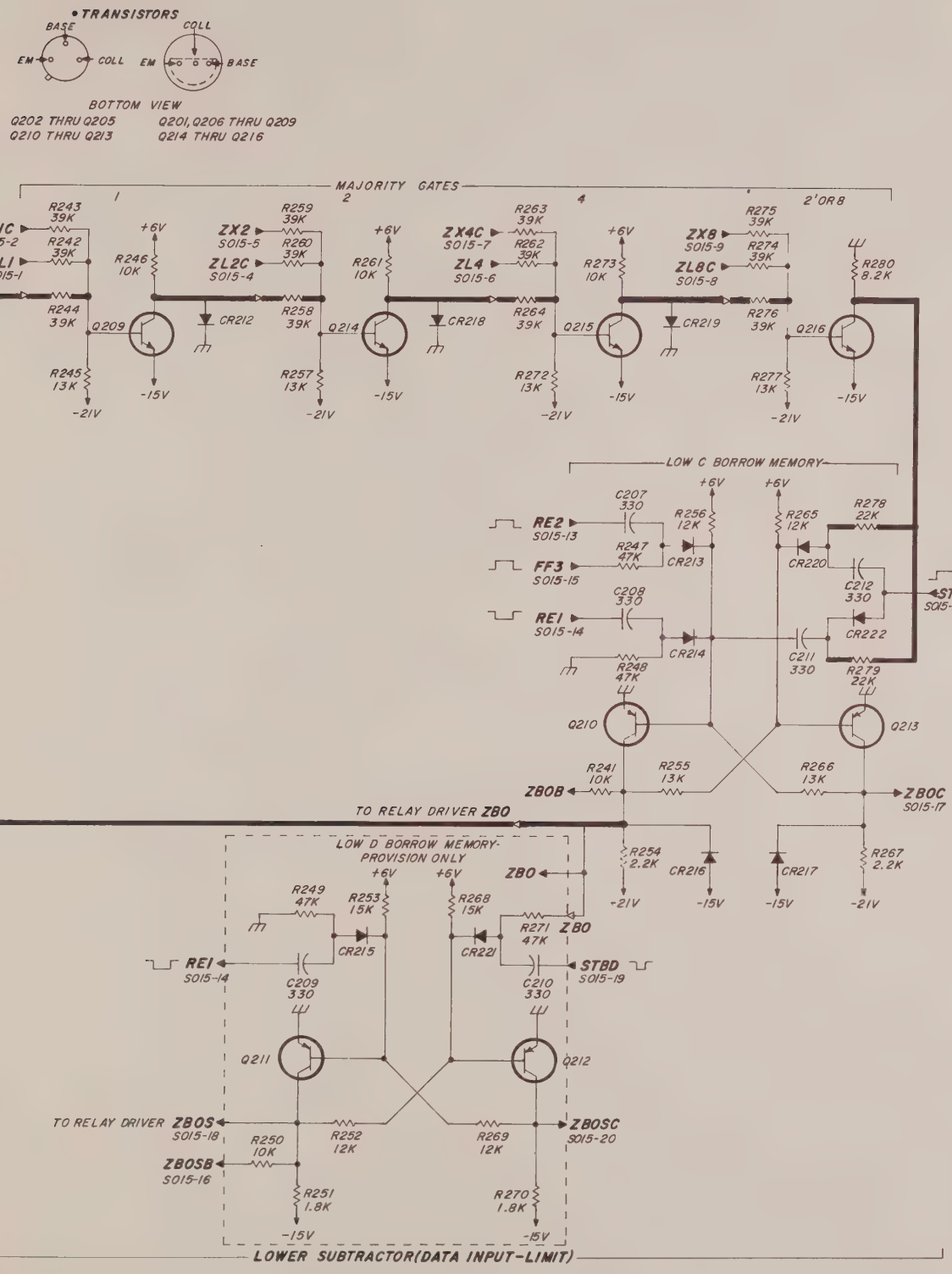
INPU
PARA

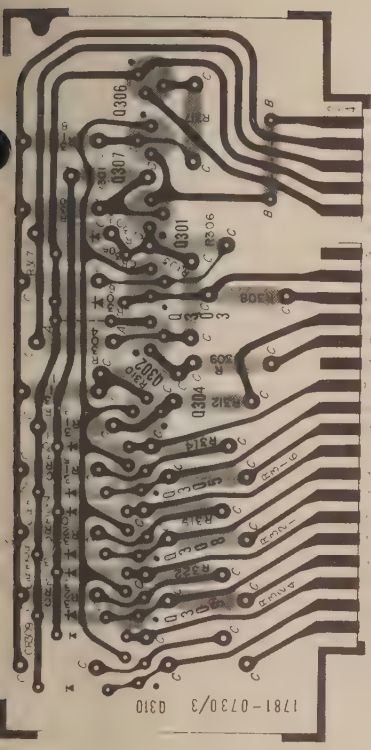
NAL DIRECTION
UTPUT TO ANOTHER DIAGRAM
IPUT FROM ANOTHER DIAGRAM
ITPUT REMAINS ON DIAGRAM
PUT FROM SAME DIAGRAM

•FLOATING GROUND
VREF (⏚) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS (SO30, 31, 32)

•LOW D
PROVISION HAS BEEN MADE FOR LOW D COMPARISONS; WIRING IS PRESENT BUT COMPONENTS ARE NOT

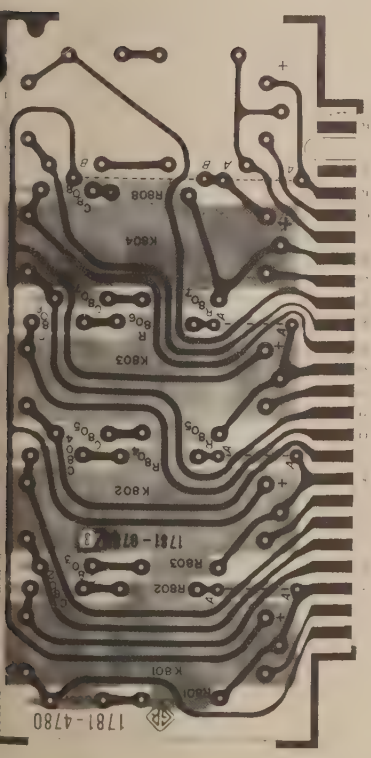



• TRANSISTORS
BASE
COLL
EM
COLL
EM
BASE
BOTTOM VIEW
Q202 THRU Q205
Q210 THRU Q213
Q201, Q206 THRU Q209
Q214 THRU Q216
MAJORITY GATES
1
2
4
2'OR8
ZX2
SO15-5
ZL2C
SO15-4
ZX4C
SO15-7
ZL4
SO15-6
ZX8
SO15-9
ZL8C
SO15-8
+6V
-15V
-21V
Q209
Q214
Q215
Q216
CR212
CR218
CR219
LOW C BORROW MEMORY
RE2
SO15-13
FF3
SO15-15
RE1
SO15-14
STB
SO15-10
CR213
CR214
CR220
CR222
Q210
Q213
ZBOB
ZBOC
SO15-17
TO RELAY DRIVER ZBO
LOW D BORROW MEMORY-
PROVISION ONLY
ZBO
CR215
CR221
CR216
CR217
STBD
SO15-19
Q211
Q212
TO RELAY DRIVER ZBOS
SO15-18
ZBOSB
SO15-16
ZBOSC
SO15-20
LOWER SUBTRACTOR(DATA INPUT-LIMIT)



S016 LEFT

1	-15V	POWER
2	-21V	POWER
3	+6V	POWER
4	VREF	FLOATING GROUND
5	LPGP	DRIVER ENABLE
6		
7	GOR	GO – RELAY DRIVE
8	GOL	GO – LAMP DRIVE
9	CKK	IN – TOLERANCE
10	CK	OUT–OF–TOLERANCE
11		
12	BO	HIGH C BORROW
13	HICR	HIGH C RELAY DRIVE
14	HICL	HIGH C LAMP DRIVE
15	ZBO	LOW C BORROW
16	LOCR	LOW C RELAY DRIVE
17	LOCL	LOW C LAMP DRIVE
18	BOS	HIGH D BORROW
19	HIDR	HIGH D RELAY DRIVE
20	HIDL	HIGH D LAMP DRIVE
21	ZBOS	LOW D BORROW
22	LODR	LOW D RELAY DRIVE
23	LODL	LOW D LAMP DRIVE



S027 RIGHT

1	15V	POWER
2		
3	6V	POWER
4	VREF (⏚)	FLOATING GROUND
5	LODR	LOW D DRIVE
6	LDC	LOW D PROVISION
7	HDC	HIGH D COMMON CONTACT
8	HIDR	HIGH D DRIVE
9	LODNO	LOW D PROVISION
10	LODNC	LOW D PROVISION
11	HIDNO	HIGH D NORMALLY OPEN CONTACT
12	LC	LOW C COMMON CONTACT
13	LOCR	LOW C DRIVE
14	HIDNC	HIGH D NORMALLY CLOSED CONTACT
15	LOCNO	LOW C NORMALLY OPEN CONTACT
16	LOCNC	NORMALLY CLOSED CONTACT
17	HC	HIGH C COMMON CONTACT
18	HICR	HIGH C DRIVE
19	HICNO	HIGH C NORMALLY OPEN CONTACT
20	HICNO	HIGH C NORMALLY CLOSED CONTACT
21	GONO	GO NORMALLY OPEN CONTACT
22	GC	GO COMMON CONTACT
23	GOR	GO DRIVE
24	GONC	GO NORMALLY CLOSED CONTACT

• SIGNAL DIRECTION
→ OUTPUT TO ANOTHER DIAGRAM
→ INPUT FROM ANOTHER DIAGRAM
→ OUTPUT REMAINS ON DIAGRAM
→ INPUT FROM SAME DIAGRAM

• FLOATING GROUND
VREF(⏚) ELEVATED FROM CHASSIS GROUND BY EXTERNAL VOLTAGE APPLIED TO PIN C12 OF REAR MOUNTED SOCKETS(SO30, 31, 32)

• LOW D
*PROVISION HAS BEEN MADE FOR LOW D COMPARISONS; WIRING IS PRESENT BUT COMPONENTS ARE NOT

• TRANSIS
BASE
EM
COLL
BOTTOM
Q302

LAMPS ARE MOUNTED ON FRONT PANEL

RELAY CIRC
1781-4780

RELAY CONTACT RATING
115V RMS
0.1A RMS

R801 120
C801 .0047
NC
GONC SO27-1
GC SO27-3
R802 120
GONO SO27-4
C802 .0047
K801
GOR SO27-2

R805 120
C805 .0047
NC
LOCNC SO27-9
LC SO27-13
R806 120
LOCNO SO27-10
C806 .0047
K803
LOCR SO27-12

P901 GO
P902 NO GO LOW C

GOR SO16-7
GOL SO16-16
LOCR SO16-8
LOCL SO16-7

+6V
R303 1.2K
R306 5.6K
R307 27K
-21V
R308 56
Q303
CR306
A (-15V)
GO DRIVER

R319 8.2K
ZBO SO16-9
R320 15K
-21V
Q308
R321 100
CR308
A (-15V)
LOW C DRIVER

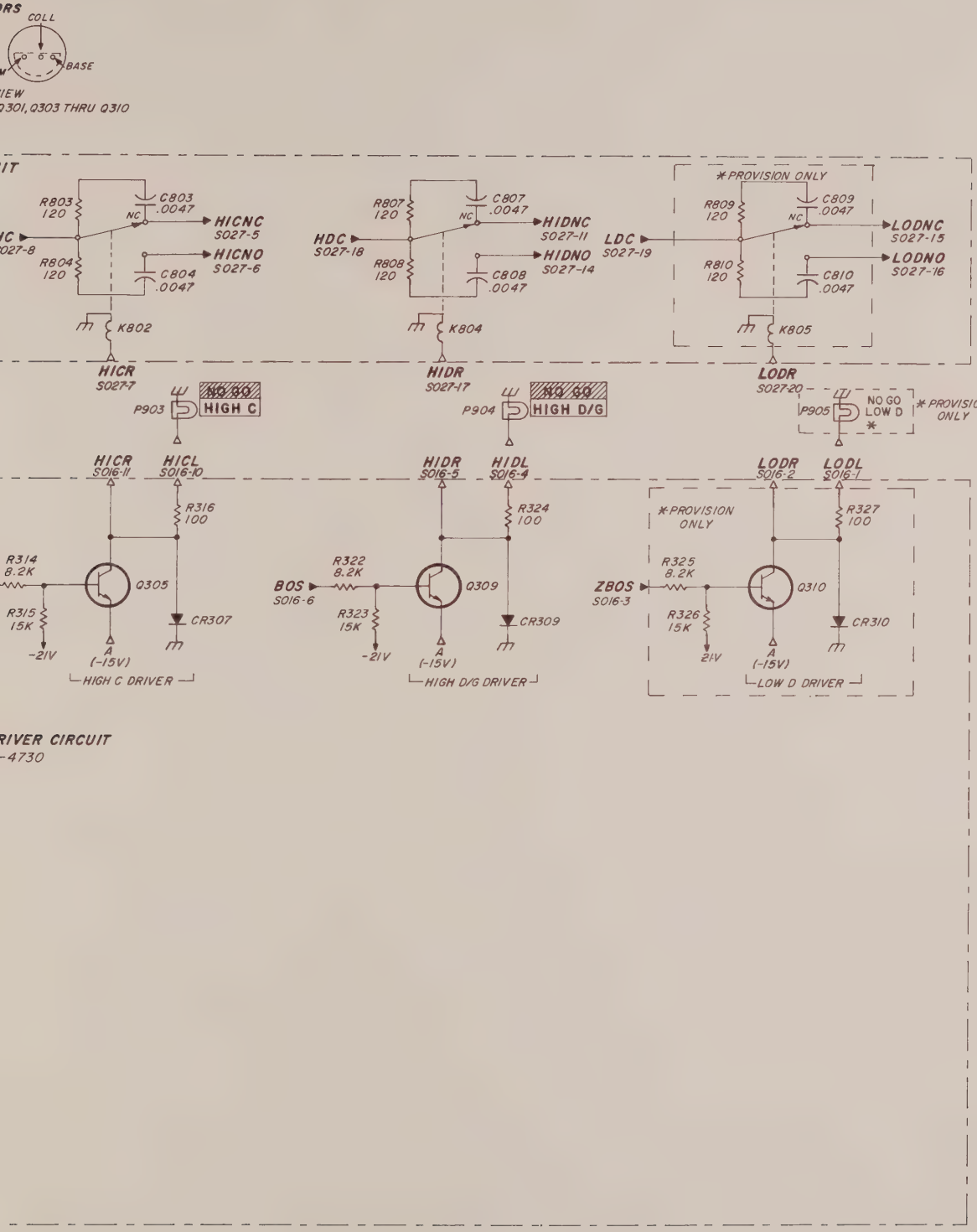
BO SO16-12

CR302
LOW C ZBO SO16-9
CR301
HIGH C BO SO16-12
CR303
HIGH D/G BOS SO16-6
CR304 *
LOW D ZBOS SO16-3
*PROVISION ONLY
R301 15K
R302 22K
-21V
-15V
Q301
CR305
NO-GO NOR GATE

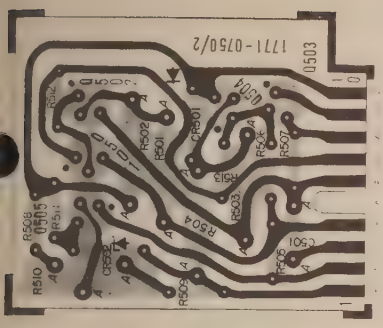
+6V
R304 10K
R305 10K
Q302
R310 5.6K
R309 1K
CK SO16-14
R311 27K
-21V
R313 2.2K
Q304
A (-15V)
R312 1K
CKK SO16-15
OUT-OF-TOLERANCE AMPLIFIER
IN-TOLERANCE AMPLIFIER

RELAY

A
LPGP SO16-20
Q306
R317 1.8K
Q307
R318 5.6K
-15V
-21V
DRIVER ENABLE AMPLIFIER

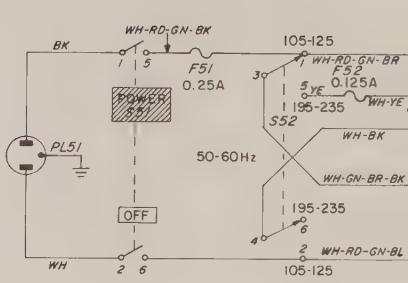


RIVER CIRCUIT
-4730

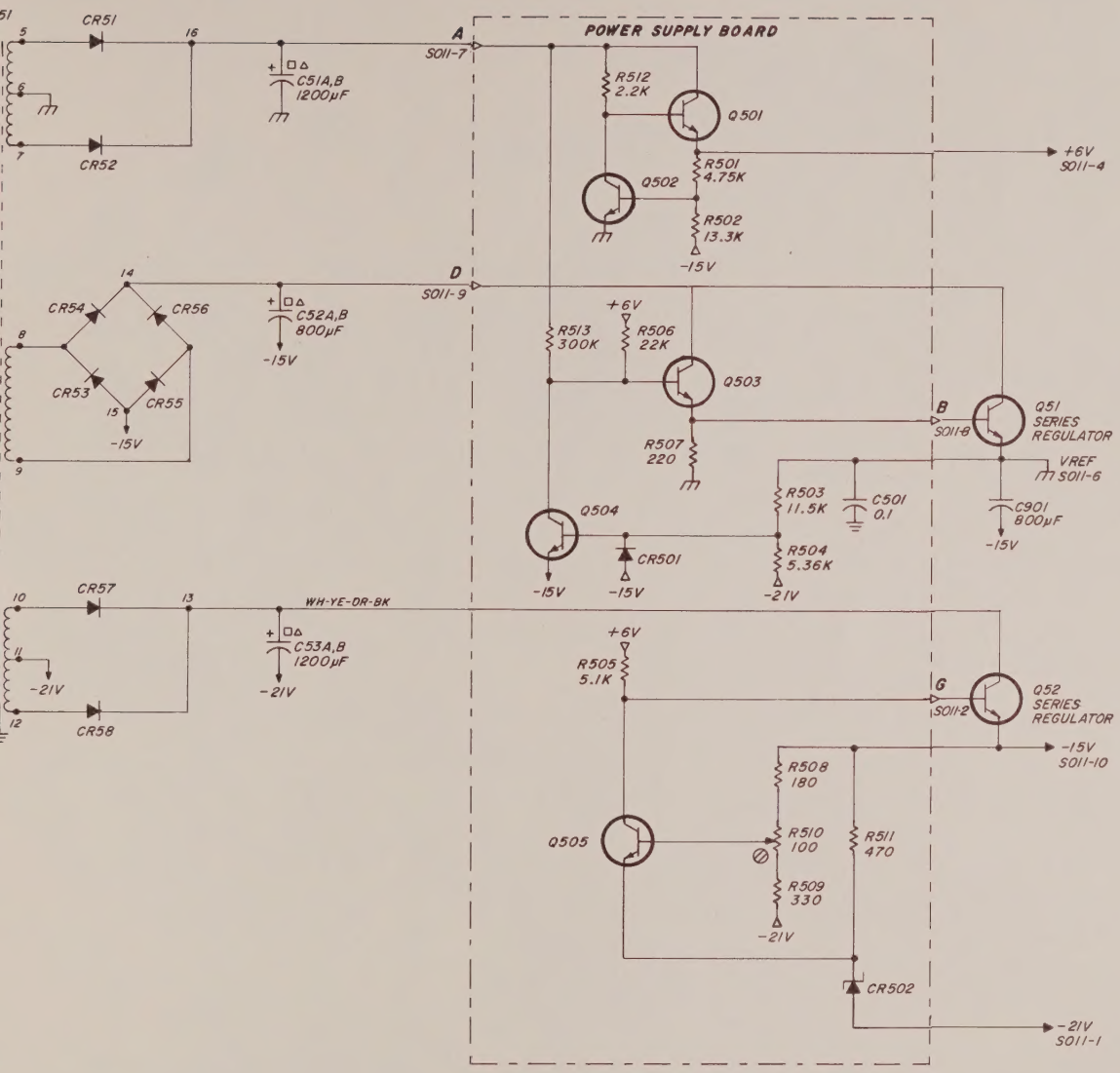


S011

1	-15V	REGULATED
2	D	UNREGULATED VREF
3	B	VREF ERROR VOLTAGE
4	A	UNREGULATED +6V
5	VREF (⏚)	FLOATING GROUND
6	6V	REGULATED
7	CGND (⏚)	CHASSIS GROUND
8	G	-15V ERROR VOLTAGE
9	21V	REGULATED



NOTE: FOR 210-250V OPERATION, CHANGE WH-YE FROM 2L TO 2


POWER SUPPLY BOARD
CR51
CR52
C51A,B 1200μF
A
S011-7
R512 2.2K
Q501
R501 4.75K
Q502
R502 13.3K
-15V
+6V S011-4
CR54
CR56
CR53
CR55
C52A,B 800μF
D
S011-9
R513 300K
+6V
R506 22K
Q503
R507 220
B
S011-6
Q51 SERIES REGULATOR
VREF S011-6
R503 11.5K
C501 0.1
C901 800μF
Q504
CR501
R504 5.36K
-21V
CR57
CR58
C53A,B 1200μF
WH-YE-DR-BK
R505 5.1K
G
S011-2
Q52 SERIES REGULATOR
-15V S011-10
R508 180
Q505
R510 100
R511 470
R509 330
CR502
-21V S011-1

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